ICEPT 2023

第二十四届电子封装技术国际会议

The 24th International Conference on Electronic Packaging Technology

August 8-11th, 2023 Shihezi · China

会议手册

Conference Program

Organized by

IMECAS

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IEEE ELECTRONICS PACKAGING SOCIETY

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CONTENTS

* 中文版议程请参考 73-123 页

WELCOME FROM THE GENERAL CHAIR

The International Conference on Electronic Packaging Technology (ICEPT) is one of the flagship conferences of IEEE EPS in China. Inaugurated in 1994, ICEPT has been successfully held 23 times in Beijing, Shanghai, Shenzhen, Xi'an, Guilin, Dalian, Chengdu, Changsha, Wuhan, Harbin, Hong Kong (China), Guangzhou and Xiamen. After 29 years of efforts, ICEPT is now recognized as one of the top four electronic packaging academic conferences, together with ECTC, ESTC and EPTC.

This year, the International Conference on Electronic Packaging Technology (ICEPT) reaches its 24th anniversary. ICEPT 2023 is locally hosted and co-organized by Shihezi University, technically sponsored by IEEE Electronics Packaging Society (EPS). In this conference, there are more than 700 delegates from 14 countries and regions with more than 500 papers covering ten special themes.

Shihezi University, the organizer of this year's conference, is a high-level comprehensive university and has made outstanding contributions to the development of our country's border areas as well as the talent cultivation since its establishment. During the preparation process of the conference, Shihezi University has put in intensive efforts to ensure the successfully held of the event, and I would like to express my gratitude to them.

In addition to the regular sessions such as short courses, keynote lectures, invited lectures, oral presentations, poster and exhibitions, we will continue to combine offline and online platforms based on the experience of previous conferences, in order to maximize the impact of the conference and provide a communication platform for professionals and researchers from both domestic and international backgrounds. I would also like to extend my deepest gratitude to the academic committee, organizing committee, and experts from ten sessions who have worked tirelessly in the promotion, manuscript review, and preparation processes of the conference.

In the stage of steady development for the global integrated circuit and packaging industry, advanced packaging has become the driving force behind the industry's growth. Research institutions and companies with an international perspective should join the fast lane of advanced packaging development as soon as possible. Based on this background, ICEPT will face the opportunities and challenges together and continue promoting exchange of ideas and co-operation among researchers and engineers, which contributes not only to domestic high-end talent training but also to global technological exchange on electronic packaging.

This year, the International Conference on Electronic Packaging Technology will be held in our magnificent Xinjiang Province for the first time, and we are waiting for the presence of old and new friends in this beautiful frontier region. I hope this premier international conference can enhance the long-term collaboration between domestic and international organizations and conferences, such as IEEE EPS, IMAPS, ECTC, ESTC and EPTC. You are highly welcomed to ICEPT 2023 and I am looking forward to your participation.

Prof. Tianchun YE
General Chair of ICEPT 2023

CONFERENCE ORGANIZERS

Hosted by

Institute of Microelectronics Chinese Academy of Sciences

Shihezi University

IEEE Electronics Packaging Society (IEEE-EPS)

Electronic Manufacturing & Packaging Technology Society of Chinese Institute of Electronics, China (CIE-EMPT)

Organized by

Mechanical and Electrical Engineering at Shihezi University

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Session 2 – Packaging Materials & Processes

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Session 3 – Packaging Design & Modeling

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Session 4 – Interconnection Technologies

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Session 5 – Advanced Manufacturing & Packaging Equipment

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Session 6 – Quality & Reliability

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Session 7 – Power Electronics & The new energy and new power system

Chairs

Huaiyu YE	Senior Researcher and Associate Professor in Southern University of Science and Technology (SUSTech)
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Yunhai WANG	Xinjiang University
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Session 8 – Optoelectronics and New Display

Chairs

Jianhua ZHANG	Prof. of Shanghai University, China
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Session 9 – MEMS Packaging

Chairs

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Ke XIAO	Shanghai Institute of Microsystems, CAS
Libo ZHAO	Xi'an Jiaotong University
Wenwen KONG	Xinjiang Institute of Physical and Chemical Technology, Chinese Academy of Sciences

Session 10 – Emerging Technologies & Applications of Electronic Technology for Artificial Intelligence

Chairs

Daquan YU	Distinguished Professor of Xiamen University, Founder of Xiamen Sky Semiconductor Co., Ltd.
Yanhong TIAN	Tenured Professor at the Harbin Institute of Technology, Vice director of the State Key Laboratory of Advanced Welding and Joining
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Guoqiang WU	Wuhan University, China
Shang WANG	Harbin Institute of Technology
Min ZHANG	Peking University ShenZhen Graduate School, China
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Changzheng LIU	Shihezi University

OVERVIEW OF CONFERENCE PROGRAM

Note: The information is only for your reference. The final conference schedule shall prevail on the date of conference.

PROFESSIONAL DEVELOPMENT COURSE			
Date	**Time**	**Room 1**	**Room 2**
Aug. 9th	10:00--13:30	*PDC-1*	*PDC-2*
	13:30--15:30	*Lunch*	
	15:30--19:00	*PDC-3*	*PDC-4*
	19:30--21:15	*Football Game*	

PLENARY TALKS		
Date	**Time**	**North District Hall**
Aug. 10th	10:00--10:30	*OPENING CEREMONY*
		PLENARY TALK
	10:30--11:00	*PLENARY TALK 1*
	11:00--11:35	*PLENARY TALK 2*
	11:40--12:15	*PLENARY TALK 3*
	12:20--12:50	*Tea Break & Networking*
	12:50--13:25	*PLENARY TALK 4*
	13:30--14:05	*PLENARY TALK 5*
	14:10--15:40	*Lunch*
	15:40--16:10	*PLENARY TALK 6*
	16:15--16:45	*PLENARY TALK 7*
	16:50--17:20	*PLENARY TALK 8*
	17:25--17:55	*Tea Break & Networking*
	17:55--18:25	*PLENARY TALK 9*
	18:30--19:00	*PLENARY TALK 10*
	19:00--19:35	*PLENARY TALK 11*
	20:00--22:00	*Welcome Dinner*

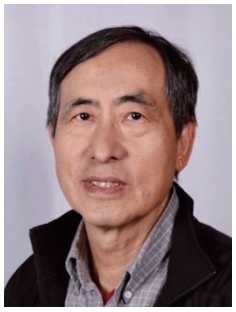
Date	**Time**	**Room 1**	**Room 2**	**Room 3**	**Room 4**	**Room 5**	**Room 6**	**Room 7**
Aug. 11th	10:00--11:45	Oral Session 1	Oral Session 2	Oral Session 3	Oral Session 4	Oral Session 5	Oral Session 6	Oral Session 7
	11:45--12:15	*Poster Session*						
	12:15--14:00	Oral Session 8	Oral Session 9	Oral Session 10	Oral Session 11	Oral Session 12	Oral Session 13	Oral Session 14
	14:00--15:30	*Lunch*						
	15:30--17:45	Oral Session 15	Oral Session 16	Oral Session 17	Oral Session 18	Oral Session 19	Oral Session 20	Oral Session 21
	17:45--18:15	*Poster Session*						
	18:15--20:30	Oral Session 22	Oral Session 23	Oral Session 24	Oral Session 25	Oral Session 26	Oral Session 27	Oral Session 28

OVERVIEW OF PROFESSIONAL DEVELOPMENT COURSE

Wednesday, August 9th, 2023 10:00--19:00 Boxue Building, Shihezi University

Venue	Time	Topic	Speaker
Room 1	10:00--11:15	***PDC-1*** Advanced Packaging Solutions for Advanced Chips	***Dr. Wei Koh*** Pacrim Technology Irvine, CA, USA
	Break		
	11:45--13:00		
	13:00--13:30	***Q&A***	
	13:30--15:30	***Lunch***	
	15:30--16:45	***PDC-3*** IEEE Heterogenous Integration Roadmap (HIR) Reliability Challenges and Roadmap	***Dr. Richard RAO*** Senior Principal Engineer at Marvell Technology, USA
	Break		
	17:15--18:30		
	18:30--19:00	***Q&A***	
Room 2	10:00--11:15	***PDC-2*** Achieving High Reliability of Lead-Free Solder Joints –Materials Considerations	***Dr. Ning-Cheng Lee*** ShinePure Hi-Tech LTD, China
	Break		
	11:45--13:00		
	13:00--13:30	***Q&A***	
	13:30--15:30	***Lunch***	
	15:30--16:45	***PDC-4*** Computer aided processes and reliability for microelectronics and packaging interaction	***Prof. Sheng LIU*** Wuhan University, China
	Break		
	17:15--18:30		
	18:30--19:00	***Q&A***	
Stadium	19:30--21:15	***Football Game***	

Introduction of PDC Lecturers



W. Koh, PhD, Pacrim Technology, Irvine, CA, USA

Dr. Koh has been working on IC packaging and microelectronics assembly technologies since the early 1980's. He has MS and PhD degrees from Cornell University and worked for Henkel, Motorola, and Kingston Technology. As a Fellow of IEEE EPS, he has over 90 publications and 40 US patents relating to microelectronics.

Course Description:

IC Backend packaging, assembly, and test (PAT) has become a practical solution for continuing Moore's Law in advancing the performance of small node semiconductors. This course will review the evolution of IC packaging technology from conventional leadframe/BGA to wafer level 3D packaging to achieve heterogeneous integration and fine-pitch, high-density interconnections. High density advanced packaging technology continues to evolve and moving forward using more complex design, new materials and high precision processes and metrology.

This course is intended for the attendees to gain understanding on the fundamentals in IC packaging technology, applications, design, materials, and manufacturing processes that are progressing in high density advanced packaging (HDAP) technology to furthering the performance of sub 10 nm advanced nodes semiconductor ICs. Specific topic discussions are focus on heterogeneous and 3D integration for wafer level fan-out, fine pitch micro-bumping and hybrid bonding, chiplet interconnection, new packaging materials and thermal management for new generation advanced packaging. Packaging examples for leading Fabs, IDMs, and OSATs are described.

Dr. Richard RAO, Senior Principal Engineer at Marvell Technology

Dr. Richard RAO is currently a Senior Principal Engineer at Marvell Technology and a Senior Member of IEEE. Prior to joining Marvell, he was a Fellow of Microsemi (Microchip) Corp and a consultant engineer at Ericson Inc. His responsibilities include the development of design for reliability flows for advanced circuits, packaging, and chip to package interaction. He was the chair of IEEE EPS (Electronics Packaging Society) Reliability Technical Committee and co-chairing the reliability roadmap for the IEEE Heterogenous Integration Roadmap. He is also the general chair and technical program chair for the IEEE REPP (Reliability of Electronics and Photonics Packaging) Symposium. He has a Ph.D. degree in solid mechanics of materials from the University of Science and Technology of China and a post-doctor research fellow at Northwestern University studying the reliability failure mechanism of advanced integrated circuits. Prior to joining Marvell, Dr. Rao held senior technical positions in reliability physics and engineering for both academia and industries. He was an assistant/associate professor at University of Science and Technology of China and a research fellow for National Science and Technology Board of Singapore.

This tutorial will focus on the following aspects of heterogenous integration reliability.

1. Introduction of heterogenous integration packages such as chiplet, 2.5D and 3D package integrations for electronics and Silicon Photonics packaging.
2. Reliability failure modes and degradation mechanisms for multi-level interconnects in the heterogenous integration system such as transistors, BEOL interconnects, TSV, uBumps, RDLs and hybrid bonding, etc.
3. Chip to package interaction reliability challenges for advanced Si nodes
4. Design for reliability
5. Qualification for reliability

Dr. Ning-Cheng Lee, ShinePure Hi-Tech LTD

Dr. Ning-Cheng Lee is founder of ShinePure Hi-Tech. Prior to that, he was the Vice President of Technology of Indium Corporation. He has been with Indium from 1986 to 2021. He received his PhD in polymer science from University of Akron in 1981, and BS in chemistry from National Taiwan University, China in 1973. Ning-Cheng is the author of "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies" by Newnes, and co-author of 5 other books. He received 1991 award from SMT Magazine and 1993 and 2001 awards for best proceedings papers of SMI or SMTA International Conferences, 2003 Lead Free Co-Operation Award from Soldertec, 2008 and 2014 awards from IPC for Honorable Mention Paper – USA Award of APEX conference, and 2010 Best Paper Award of SMTA China South Conference. He was honored as 2002 Member of Distinction from SMTA, 2006 Exceptional Technical Achievement Award from CPMT, 2007 Distinguished Lecturer from CPMT, 2009 Distinguished Author from SMTA, 2010 Electronics Manufacturing Technology Award from CPMT, 2015 Founder's Award from SMTA, and 2017 IEEE Fellow.

Course Description:

This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions, and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in detail. The selection of novel alloys with reduced fragility will be presented. Crucial parameters for high reliability solder alloy for automotive industry will be presented. Electromigration, and tin whisker growth will also be discussed. The emphasis of this course is placed on the understanding of how the numerous factors contribute to the failure modes, and how the selection of proper solder alloys and surface finishes for achieving high reliability are key.

Prof. Sheng LIU, Wuhan University, China

Prof. Sheng LIU is the dean of the School of Power and Mechanical Engineering and the Institute of Technological Science of Wuhan University. He is the National Science Fund for Distinguished Young Scholars (Type B), Yangtze River Scholar Distinguished Professor, ASME Fellow, IEEE Fellow, and as a professionalism in the area of the "863 program" of the National High Technology Research and Development Program. He has acquired his doctor degree in Stanford University in 1992. From 1992 to 1995, he held the title of lecturer at Florida institute of technology. He was authorized as a tenure from 1995 to 2001 in the Department of Mechanical Engineering and manufacturing research at Wayne State University. During the period of his title job, he was granted the President's prize of USA. The research of IC and MEMS packaging with the research of CAD allowed him to obtain the Young Investigator Award in Natural Sciences of the United States of America. In 2001, Liu Sheng resigned from the Department of Mechanical Engineering and Manufacturing research at Wayne State University and returned to China, where he took the lead of carrying out research focusing on the theory of Reliable Engineering Development for LED electronic packaging.

OVERVIEW OF PLENARY TALKS

Thursday, Aug. 10th, 10:00--19:35 North District Hall, Shihezi University

OPENING CEREMONY **Chair: Prof. Kouchi ZHANG, Delft University of Technology, Netherlands**	
10:00--10:30	**Welcome Addresses** *Prof. Tianchun YE*, Chair of ICEPT *Prof. Bin DAI*, President of Shihezi University *Leader* from Shihezi City *Dr. Kitty PEARSALL*, President of IEEE EPS
PLENARY TALKS **Chair: Prof. Xuejun FAN, Lamar University, USA**	
10:30--11:00	**Supply Chain Trends, Challenges, and Disruptions in Semiconductor Packaging** *Dr. Kitty PEARSALL* President of IEEE EPS
11:00--11:35	**Revolution of Microsystem Integration by Innovations in High Performance Packaging** *Mr. Li ZHENG* CEO of JCET Group Co., Ltd.
11:40--12:15	**Surface Activated Bonding (SAB) for Low-Temperature 3D Integration** *Prof. Tadatomo SUGA* Professor Emeritus of the University of Tokyo, Professor of Meisei University
12:20--12:50	*Tea Break & Networking*
12:50--13:25	**Metal Thin Film Equipment and Process Challenges in Advanced Packaging** *Mr. Bo GENG* Deputy General Manager of The PVD BU, Beijing NAURA Microelectronics Equipment Co., Ltd.
13:30--14:05	**The Localization Trends and Challenges on Advanced Packaging Technology** *Mr. Cheng LI* Hygon Information Technology Co., Ltd.
14:10--15:40	*Lunch*
Chair: Prof. Ricky LEE, Hongkong University of Science & Technology, China	
15:40--16:10	**Holistic ESD Protection Co-Design: Challenges** *Prof. Albert Z Wang* Director, Center for Ubiquitous Communication by Light (UC-Light), University of California, Riverside
16:15--16:45	**Manufacturing Technologies of Heterogeneous Integration for In-memory Computing** *Dr. Koukou Suu* Executive Officer and Senior Fellow, ULVAC, Inc. President & CEO, ULVAC Technologies Inc.
16:50--17:20	**Hybrid bonding for next generation advanced interconnection technologies** *Dr. Anton Alexeev* Business Development Manager of EV Group
17:25--17:55	*Tea Break & Networking*

17:55--18:25	**CPO Status and Technologies** *Ms. Yuan ZHANG* Senior Teacher
18:30--19:00	**Paradigm Change of Design Rules from Electromigration to Thermomigration / Electromigration** *Prof. Xuejun FAN* Lamar University, Beaumont, TX
19:05--19:35	**Advanced Packaging for Chiplet** *Dr. Qidong WANG* Director of National Center of Advanced Packaging, IME-CAS
20:00--22:00	*Welcome Dinner* *Grand link hotel, Shihezi*

INTRODUCTION OF INVITED PLENARY KEYNOTE SPEAKERS

Dr. Kitty PEARSALL, IEEE EPS President

Dr. Kitty PEARSALL received the BS degree in Metallurgical Engineering and her MS and PhD degrees in Mechanical Engineering and Materials from the University of Texas. Across her 41-year career at IBM, Kitty was appointed to increasingly strategic roles and received multiple awards for her work. Currently Kitty is President of Boss Precision Inc. and works as an independent consultant.

- IBM Distinguished Engineer in Integrated Supply Chain, Retired
- Emeritus Member of IBM Academy of Technology
- PE for State of Texas since 1993
- Twelve US patents; and 8 published disclosures
- Numerous internal IBM publications as well as 24 external publications
- UT Austin – Cockrell Engineering Distinguished Engineering Graduate Award (2007)
- UT Mechanical Engineering Dept. Academy of Distinguished Alumni
- IBM Women in Technology Fran E. Allan Mentoring Award (2008)
- Active IEEE member for 31 years; EPS/CPMT member for 28 years
- BOG member since 2006 serving in various roles

Mr. Li ZHENG, CEO of JCET

Mr. Li ZHENG is a member of the board of directors and Chief Executive Officer at JCET Group Co., Ltd. JCET Group is a leading global semiconductor system integration packaging and test provider, offering a full range of turnkey services that include semiconductor package integration design and characterization, R&D, wafer probe, wafer bumping, package assembly and final test.

Prof. Tadatomo SUGA, Professor Emeritus of the University of Tokyo, Professor of Meisei University

Prof. Tadatomo SUGA joined the Max-Planck Institute für Metallforschung in 1979, obtained his Ph.D. degree in materials science from University of Stuttgart in 1983. Since 1984 he has been a faculty member of the University of Tokyo and a professor in the Department of Precision Engineering of the School of Engineering since 1993. He was also the director of the Research Group of Interconnect Eco-design at the National Institute of Materials Science (NIMS), a Member of the Japan Council of Science, and the Chair of IEEE CPMT Society Japan Chapter, as well as the President of the Japan Institute for Electronic Packaging (JIEP). His research focus on microsystems integration and packaging and developing interconnect technology, especially the room temperature bonding technique for 3D integration. He has endeavored to establish collaboration between industries and academia for packaging technology, direct the R&D project of the Institute of Micro System Integration (IMSI), and advocate the importance of the environmental aspects of packaging technology as the key organizer of the International Eco-design Conference.

Mr. Bo GENG, Deputy General Manager of The PVD BU, Beijing NAURA Microelectronics Equipment Co., Ltd.

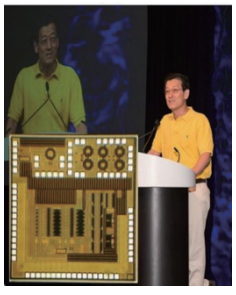
Mr. Bo GENG is the deputy general manager of PVD BU in NAURA. He received the M.S. degree in plasma physics from Hebei University and joined NAURA in 2010. He has led the development of several PVD equipments for IC, advanced packaging, power devices, LED applications. He has been awarded more than 20 patents.

Mr. Cheng LI, Hygon Information Technology Co., Ltd.

Mr. Cheng LI graduated from Southeast University majored in Electronic Engineering. Around 20 years' experience in semiconductor industry, especially the expertise in Fairchild/AMD from discrete device to logic IC. Longly focus on 2.5D advanced packaging start from 2010 to develop engineering prototype with interposer technology, leading 2.5D testing & FA methodology initiatives. Leaded & covered CPU & GPU NPI work from post-silicon point of view with generations of leading-edge process nodes experience. Recently put major efforts on localization for IC design & manufacturing related supply chain. Have integrated related supply chains from Mainland to assemble interposer 2.5D product & Fanout product, both comparable with abroad technology from package size & performance point of view. Continue the efforts to move to more localization areas including EDA & IP.

Speech Description:

Advanced packaging technology is moving fast from both engineering & manufacturing sides in abroad, and recent years, the Domestic manufacturer is putting heavy efforts on this area as well with fast iteration. The late-development advantages from capital & talent sides will accelerate Domestic process development, and also the IC design house will have a better view on technology commercialization to screened out those with high-chance to success. This paper will focus on different methods to make a "2.5D" product from with both interposer & Fanout RDL efforts, we have co-worked & developed such product with local supply chains, all good to work. We will also focus on 3D, the challenge will even bigger, but from design house point of view, the challenge from product design, definition, post silicon logic is also giant, need to put all of these considerations systematically, we may then fully utilize the advance from advanced packaging.



Prof. Albert Z Wang, Director, Center for Ubiquitous Communication by Light (UC-Light), University of California, Riverside

Albert Z Wang is a Professor of Electrical and Computer Engineering at University of California, Riverside, USA. His research covers semiconductor devices, analog/mixed-signal and RF ICs, design-for-reliability for ICs, 3D heterogeneous integration, emerging devices and circuits, and LED visible light communications. He published two books and 310+ peer-reviewed papers, and holds sixteen U.S. patents. He has been IEEE Distinguished Lecturer for IEEE Electron Devices Society, IEEE Circuits and Systems Society and IEEE Solid-State Circuits Society. He was President of IEEE Electron Devices Society. He served as a Program Director of the National Science Foundation, USA. He was recipient of IEEE J. J. Ebers Award. Wang is a Fellow of National Academy of Inventors and an IEEE Fellow.

Speech Description:

Electrostatic discharge (ESD) protection has been a major reliability problem for integrated circuits (IC) and microelectronics systems, including bare dies and packaged microchips. Any on-chip/in-package/on-board ESD protection will inevitably affect system performance. On the other hand, 3D heterogeneous integration (HI) technologies and hetero-integrated microsystems lead to new complexity in ESD protection designs. Holistic ESD protection co-design hence becomes essential to advanced microsystem chips. This paper highlights key emerging ESD protection design challenges and discusses some ESD protection perspectives for future chips.

Dr. Koukou Suu, Executive Officer and Senior Fellow, ULVAC, Inc. President & CEO, ULVAC Technologies Inc.

Dr. Koukou Suu graduated and received Ph.D. degree in Engineering from Tohoku University, Japan in 1988 and 1993 respectively. He joined ULVAC, Inc. in 1993 and since then has been leading and engaging with developments of numerous semiconductor and electronics technologies including emerging non-volatile memories, high-K capacitors, LED, power devices, thin-film Li-battery as well as 3D packaging manufacturing technologies. He was General Manager of Institute of Semiconductor and Electronics Technologies of the company from 2008 to 2014. Currently he is Executive Officer and Senior Fellow of ULVAC, Inc. as well as President and CEO of ULVAC Technologies, Inc, a company representing ULVAC in North America. He is also an Adjunct Professor of Shanghai Institute of Microsystem and Information Technology of Chinese Academy of Science as well as an Adjunct Industrial Professor of University of South Australia. He has contributed to over 170 Patents (Japan, EU, US) and more than 80 industry & academic publications.

Dr. Anton Alexeev, Business Development Manager of EV Group

Dr. Anton Alexeev is Business Development Manager at EV Group, where he focuses on wafer bonding technologies for a variety of 3D and heterogeneous integration applications. Anton received his PhD in electrical engineering from the Eindhoven University of Technology where he also graduated Professional Doctorate in Engineering program in physics. He has years of professional experience in the semiconductor industry. He worked on variety of technologies ranging from visible light communication via LED with Philips Lighting to optimization of the overlay performance for the leading-edge semiconductor manufacturing nodes with ASML.

Speech Description:

Hybrid wafer-to-wafer bonding gained over the past decade a significant interest as it can provide major advantages in fabrication of wafer-level interconnects. As an alternative process, die-to-wafer process flows were developed. Such approach is based on the principle of known good die: after wafer fabrication the dies are going through dicing and the dies passing the quality criteria are used to bond on a wafer. In this way, the bonding yield loss due to the individual wafers' yield loss is minimized.

An overview of the two types of hybrid bonding will be presented. Two types of die-to-wafer process flows will be introduced. The main specifications and some of the main challenges of this technology will be reviewed with respect to their impact on process results. The importance of new metrology and investigation methods adoption will be emphasized.

Ms. Yuan ZHANG, Senior Teacher

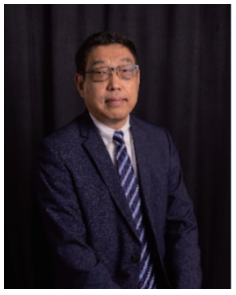
Ms. Yuan ZHANG has worked in Huawei over twenty years, as an expert on advanced material and process R&D. In 2020, She left Huawei and has been engaged in part time training activities.

Speech Description:

In this presentation, the concept understanding of CPO/NPO/LPO will be introduced. Then it will present the advantages of the potential products. In this talk, it will cover the CPO history, status and trends information from mainstream companies. And what key technologies including in CPO or NPO will be introduced too. At last, the speaker is going to analyze the supply chain challenges and relative standard work.

Outline:

1. The concept understanding of CPO/NPO/LPO
2. The advantages of the potential products
3. The CPO history, status and trends
4. The technologies including in CPO or NPO
5. The supply chain challenges and relative standard work



Prof. Xuejun FAN, Lamar University, Beaumont, TX

Xuejun FAN is a Regents' Professor of Texas State University System, and a Mary Ann and Lawrence E. Faust Endowed Professor at Lamar University, Beaumont, Texas. Dr. Fan is an IEEE Fellow, and an IEEE Distinguished Lecturer. He received the Outstanding Sustained Technical Contribution Award in 2017, and the Exceptional Technical Achievement Award in 2011 from Electronic Packaging Society of IEEE. Dr. Fan is a co-chair of Modeling and Simulation in Heterogeneous Integration Roadmap committee.

Speech Description:

As demand for high-performance semiconductors increases, heterogeneous integration using a combination of 3D monolithic and 2.5D/3D advanced packaging technology can boost the system performance significantly. Consequently, electromigation (EM)-induced failure in micro-bumps and redistribution lines (RDL) has become a great concern. In addition, thermomigration (TM) due to Joule heating, combined with EM, is becoming of the potential risks in future micro-/nano-electronics. In this presentation, I will present some general guidelines about design rules and accelerated tests for electromigration (EM)-induced failure, based on fully coupled modeling. For years, the existing EM theories have succeeded only in partially predicting or explaining complicated phenomena in experiments. Recently, we sorted out many incorrect models and assumptions under the framework of the coupling theory. In addition, taking multi-scale effects into consideration, we used molecular dynamics simulation to determine the key microscopic parameters, thus establishing a complete and self-consistent multi-physics coupling model of electromigration. We further conducted extensive EM tests and collected consistent test data for the purpose of model verification. The theoretical and numerical results fully reproduced the various phenomena in the experiments, including the impact of thermomigration. We then used the validated theory to provide new insights into design rules and acceleration factors to prevent EM-induced failure.

Dr. Qidong WANG, Director of National Center of Advanced Packaging, IME-CAS

Dr. Qidong WANG received his B.S. degree in Electronics Engineering from Southeast University in Nanjing, MSc degree from Nottingham University in UK, Ph.D. degree in Microelectronics and Solid-State Electronics from University of Chinese Academy of Sciences. He worked in Varian Lab, Stanford University as a Visiting Scholar from 2015 to 2016. He currently serves as the Director of Packaging and Integration R&D Center in the Institute of Microelectronics of the Chinese Academy of Sciences. He has been the Principal Investigator in multiple National Science and Technology Major Programs, and he is the author of more than 60 internationally referred journal and conference papers including Nature, TAP, AWPL, Physics Review A etc., and 76 filed patents. His research interests include Heterogeneous Integration, Antenna-in-Package, 2.5D/3D integration, and Advanced Substrate.

OVERVIEW OF ORAL PRESENTATION SESSIONS

Friday, August 11th, 2023 10:00--20:30 Boxue Building, Shihezi University

<table>
<tr><th></th><th>Room 1</th><th>Room 2</th><th>Room 3</th><th>Room 4</th><th>Room 5</th><th>Room 6</th><th>Room 7</th></tr>
<tr><td>10:00--11:45</td><td>Oral Session 1
Session 1</td><td>Oral Session 2
Session 2</td><td>Oral Session 3
Session 3</td><td>Oral Session 4
Session 4</td><td>Oral Session 5
Session 6</td><td>Oral Session 6
Session 8&9</td><td>Oral Session 7
Session 7</td></tr>
<tr><td>Chair</td><td>Qidong WANG</td><td>Xu LONG</td><td>Daoguo YANG</td><td>Chenxi WANG</td><td>Bin XIE</td><td>Jianhua ZHANG</td><td>Huaiyu YE</td></tr>
<tr><td>10:00--10:30
Keynote</td><td>Cheng-Tar Terry WU</td><td>Guoping ZHANG</td><td>Ziyu LIU</td><td>Qian WANG</td><td rowspan="2">46, 70, 91,
104, 185, 198,
210</td><td>Weisu CHEN</td><td>Haibo FAN</td></tr>
<tr><td>10:30--11:45
Oral</td><td>23, 54, 55,
87, 125</td><td>21, 34, 35, 78</td><td>22, 24, 28,
42, 45</td><td>119, 149, 189,
190, 200</td><td>138, 151, 179,
279, 403</td><td>247, 387, 624
Jing ZHANG
(11:15--11:45)</td></tr>
<tr><td>11:45--12:15</td><td colspan="7">Poster Session</td></tr>
<tr><td>12:15--14:00</td><td>Oral Session 8
Session 1</td><td>Oral Session 9
Session 2</td><td>Oral Session 10
Session 3</td><td>Oral Session 11
Session 4</td><td>Oral Session 12
Session 6</td><td>Oral Session 13
Session 9&10</td><td>Oral Session 14
Session 7</td></tr>
<tr><td>Chair</td><td>Shenglin MA</td><td>Zhiquan LIU</td><td>Xiangmeng JING</td><td>Yingxia LIU</td><td>Xiaofeng YANG</td><td>Jintang SHANG</td><td>Hongwei LIANG</td></tr>
<tr><td>12:15--12:45
Keynote</td><td>Wei WANG</td><td>Ning DA</td><td>Zhong TIAN</td><td rowspan="2">202, 204, 220,
221, 301,319,
417</td><td rowspan="2">264, 292, 307,
320, 326, 386, 420</td><td>Scott CHEN</td><td>Chuantong CHEN</td></tr>
<tr><td>12:45--14:00
Oral</td><td>216, 260, 282,
360, 501</td><td>97, 113, 130,
133, 206</td><td>57, 69, 79,
94, 117</td><td>64, 98, 122,
134, 146</td><td>323, 553, 621
Bin WANG
(13:30--14:00)</td></tr>
<tr><td>14:00--15:30</td><td colspan="7">Lunch</td></tr>
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15:30--17:45	Oral Session 15 Session 1&5	Oral Session 16 Session 2	Oral Session 17 Session 3	Oral Session 18 Session 4	Oral Session 19 Session 6	Oral Session 20 Session 10	Oral Session 21 Session 2
Chair	**Wei WANG**	**Yunwen WU**	**Tao HANG**	**Ziyu LIU**	**Bin XIE**	**Daquan YU**	**Yujie LI**
15:30--16:00 Keynote	**Linling CAI**	**Zheng HAN**	148, 153, 186, 240, 290, 293, 311, 341, 350	**Li GONG**	421, 467, 472, 514, 526, 528, 533, 598, 643	**Wenbiao RUAN**	**Yunhui MEI**
16:00--17:45 **Oral**	**Daping YAO (16:00--16:30)** **Yun CHEN (16:30--17:00)** 513, 604, 147	234, 241, 246, 263, 265, 277, 327		424, 425, 441, 450, 451, 457, 463		233, 274, 276, 284, 354, 382, 460	482, 517, 536, 540, 544, 586, 590
17:45--18:15	Poster Session						
18:15--20:30	Oral Session 22 Session 1&5	Oral Session 23 Session 2	Oral Session 24 Session 3	Oral Session 25 Session 4	Oral Session 26 Session 6&7	Oral Session 27 Session 10	Oral Session 28 Session 2&3
Chair	**Sheng LIU**	**Liyin GAO**	**Fengman LIU**	**Yu ZHANG**	**Min LU**	**Yanhong TIAN**	**Caifu LI**
18:15--18:45 Keynote	**Richard RAO**	328, 329, 333, 338, 351, 367, 388, 432, 437	400, 406, 408, 512, 585, 626, 664, 684, 695	471, 473, 522, 525, 599, 610, 660, 669	671, 694, 701, 709, 724, 731, 736, 443, 452	**Hongjun JI**	629, 646, 722, 440, 442, 717, 726, 730
18:45--20:30 **Oral**	238, 275, 324, 435, 490					618, 662, 677, 737	

OVERVIEW OF POSTER SESSIONS

<table>
<tr><th colspan="14">Poster Session
Friday, August 11th, 2023 (11:45--12:15/17:45--18:15)</th></tr>
<tr><th colspan="2">Area1</th><th colspan="2">Area2</th><th colspan="2">Area3</th><th colspan="2">Area4</th><th colspan="2">Area5</th><th colspan="2">Area6</th><th colspan="2">Area7</th></tr>
<tr><td colspan="2">Session 1
Advanced Packaging

Session 2
Packaging Materials & Processes</td><td colspan="2">Session 3
Packaging Design & Modeling

Session 4
Interconnection Technologies</td><td colspan="2">Session 5
Advanced Manufacturing & Packaging Equipment

Session 6
Quality & Reliability</td><td colspan="2">Session 7
Power Electronics & The new energy and new power system

Session 8
Optoelectronics and New Display</td><td colspan="2">Session 9
MEMS Packaging

Session 10
Emerging Technologies & Applications of Electronic Technology for Artificial Intelligence</td><td colspan="2">Session 2
Packaging Materials & Processes</td><td colspan="2">Session 1
Advanced Packaging

Session 2
Packaging Materials & Processes</td></tr>
<tr><td>255, 303, 322, 361, 449, 454, 492, 515</td><td>4, 44, 67, 88, 92, 129, 163, 227</td><td>10, 56, 135, 140, 142, 150, 222, 224</td><td>33, 90, 401, 462, 551, 659, 704, 706</td><td>195, 209, 219, 237, 262, 280, 287, 296</td><td>6, 12, 32, 37, 48, 63, 72, 73</td><td>11, 76, 80, 121, 235, 244, 332, 357</td><td>20, 89, 131, 249, 251, 306, 316, 317</td><td>384, 465, 582, 708, 728</td><td>5, 15, 167, 191, 225, 429, 487, 510, 511, 587, 592</td><td>228, 229, 231, 253, 295, 304, 308, 321, 335, 353, 364, 399, 404, 407, 413, 439</td><td>549, 559, 563, 603, 651, 698, 741</td><td>504, 519, 529, 613, 614, 687, 688, 689, 690</td></tr>
<tr><th colspan="14">Poster Session
Friday, August 11th, 2023 (11:45--12:15/17:45--18:15)</th></tr>
<tr><th colspan="2">Area8</th><th colspan="2">Area9</th><th colspan="2">Area10</th><th colspan="2">Area11</th><th colspan="3">Area12</th><th colspan="2">Area13</th><th></th></tr>
<tr><td colspan="2">Session 3
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Quality & Reliability</td><td colspan="3">Session 2
Packaging Materials & Processes

Session 3
Packaging Design & Modeling

Session 6
Quality & Reliability</td><td colspan="2">Session 6
Quality & Reliability</td><td></td></tr>
<tr><td>248, 346, 398, 405, 438, 448, 481, 530, 570, 573, 639</td><td>707, 711 712, 713, 718</td><td>325, 391, 392, 561, 627, 665, 679, 681</td><td>74, 81, 103, 124, 145, 152, 173, 194</td><td>446, 566, 628, 680, 693, 700, 715, 723, 746</td><td>380, 602, 620, 729</td><td colspan="2">196, 217, 250, 252, 267, 269, 352, 355, 362, 365, 369, 394, 395, 396, 412, 415</td><td>703, 721, 742, 744, 747</td><td>655, 656, 685, 714</td><td>645, 653, 657, 696, 702, 27</td><td colspan="2">418, 436, 447, 455, 456, 475, 503, 527, 548, 550, 555, 558, 581, 595, 607, 632</td><td></td></tr>
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INTRODUCTION OF INVITED SESSION KEYNOTES SPEAKERS

Dr. Cheng-Tar Terry WU, Director of Samsung Electronics

Dr. Cheng-Tar Terry WU is currently working as Director of Business Development Team, AVP, Samsung Electronics. Prior to joining Samsung, he was CTO of Chengdu ESWIN System IC. He had also held several key positions in SJSemi and TSMC. Wu received DPhil in Inorganic Chemistry from Oxford University, and MS & BS degree in Chemical Engineering from National Taiwan University, China & National Chung Hsing University, China, respectively. Dr. Wu was granted several awards in recognition of his contribution in Advanced Packaging, including 2018 Jiangsu Innovative & Entrepreneurial Talent Award, 2019 Wuxi Taihu Talent Award, 2021 Chengdu Golden Panda Talent Program, and 2022 CSTIC Best Young Engineer Award from SEMICON China. He has 14 journal and conference papers, with over 660 citations and H-index of 11. He also holds 40 US patents and 144 China patents on microelectronic packaging.

Speech Description:

With the ever-increasing demand for computing performance for mobile, IoT, AI, Big Data and automotive applications, the need for new solutions is growing due to the slowdown of Moore's Law and computing power solutions. Chiplets and advanced packaging are the key platforms to enable higher bandwidth and density for HPC and AI systems. This presentation will discuss how advanced packaging is enabling next generation computing and communication.

Prof. Wei WANG, Peking University

Prof. Wei WANG is the deputy dean of School of Integrated Circuits, Peking University and the director of the National Key Laboratory of Science and Technology on Micro/ Nano Fabrication. He received his B.S. in Thermal engineering from University of Shanghai for Science and Technology (USST, 1999) and the Ph.D. in Thermal Engineering from Tsinghua University (2005). He was a Visiting Professor in UC Davis (with Prof. Tingrui Pan) from 2007-2008 and Caltech (with Prof. YC Tai) from 2014-2015. His research focus is Parylene MEMS, clinical micro/nano system, and thermal management of 3D microsystem. He has published over 100 peer-reviewed articles, over 50 presentations with over 15 invited presentations, and 15 patents pending or granted. He is the Associated Editor of Microfluidics and Nano fluidics, Microsystems & Nanoengineering, and has served/ is serving on organizing committees for several international conferences, including IEEE MEMS '2015 and '2016, Transducers '2019, and 2021 etc.

Speech Description:

Aiming at the demand for high-density interconnection in chiplet advanced packaging, the research on chiplet embedding reconfiguration wafer with sub-micron precision, low damage and high flatness of polymer flattening, and high-density silicon-based fan-out wiring process has been carried out. It solves the ultra-thin wafer (<50μm) low-stress thinning, high-precision (±2μm) lossless wafer cutting, chip embedding with sub-micron precision (<0.5μm), ultra-low porosity (<95%) high aspect ratio trench filling, ultra-low TTV (<1μm) reconstructed wafer surface polarization, and multi-layer high-density wiring problem. Finally, a multi-layer 2μm/2μm line-width/line-space silicon fan-out wiring technology was realized, which is expected to be applied to Chiplet advanced packaging technology.

Ms. Linling CAI, Business Development Manager Thermo Fisher Scientific

Linling CAI is working for Thermo Fisher Scientific as PFA business development manager. She has more than ten years' experience of customer application supporting work of PFA systems including the failure analysis in semiconductor industry. Being familiar with the theory and application of electron microscopy, she has supported many customer's failure analysis cases for multifarious products including logic, memory, display, power device, packaging, and others. Based on her better understanding combining with the experience in application, she has provided various solution from EFA to PFA workflow to customers in different segments such as fabless, foundry, packaging house and others.

Speech Description:

Advanced packaging complexity continues to grow because of requirement for thinner, smaller, and more integrated IC products. This rising level of complexity introduces a wide range of integration challenges and associated defects. To identify the root cause of these defects, drive up yields and understand customer returns, more effective localization techniques are needed for failure analysis. Fortunately, Thermo Fisher has full FA workflow of EFA to PFA for advanced packaging. Lock-in Thermography (LIT) has been successfully demonstrated as a non-destructive analysis technique to locate the small defect. Furthermore, the high throughput FIB-SEM system can help find the defect under the surface and analyze the defects with high resolution by SEM and can provide 3D reconstruction precisely and efficiently. In this presentation, we will introduce our lock in thermography &dual beam & SEM systems with case studies to failure analysis in advance packaging.

Dr. Daping YAO, Chairman & CEO of Jiangsu CAS Microelectronics Integration Technology Co. Ltd.

Dr. Daping YAO is the founder of Jiangsu CAS Microelectronics Integration Technology Co. Ltd (Casmeit). Currently he serves as the Chairman of Board and General Manager for the company, which was established in March 2018 in Xuzhou city of Jiangsu province. After coming back from the US in June 2017, he joined the National Center for Advanced Packaging (NCAP) and had been responsible for various R&D projects of wafer level packaging technologies including TSV integration and FOWLP. He also bestowed a senior Principal Investigator of Jiangsu Industrial Technology Research Institute. Casmeit has been founded to be a high-volume production facility dedicated to advanced packaging. Over last a few years, the company has built the capabilities covering a variety of advanced packaging technologies, including wafer level high-density packaging, 3D system integration, system-in-package, and numerous other generic packaging technologies. Dr. Yao had worked for Applied Materials Inc California, USA for more than 20 years. His professional experience covers various areas including the development of semiconductor manufacturing processes, process integration, and equipment systems. Dr. Yao holds Ph. D. in Materials Science and Engineering from the University of Illinois at Urbana-Champaign, USA.

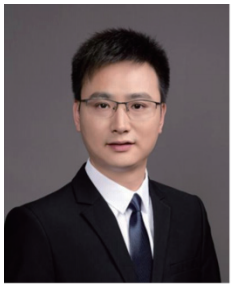
Speech Description:

It is well known that die or wafer stacking technologies are currently the main solutions that can meet the required performance of applications such as artificial intelligence (AI) and big data center. The most popular stacking integration technologies on the market are based on TSV interposer and TSV-less RDL interconnect for chiplets through heterogeneous integration. Currently, for example HBM and CIS are widely used through silicon via (TSV) technology. The recently emerged TSV-less technology consists of two groups: "with substrate" and "embedded in substrate". Hybrid bonding can bridge the two main categories of "with TSV" and "without TSV". This popular technique can be a complimentary or competition to TSV technology.

As building blocks to complicated heterogeneous packages, wafer level fanout technology and TSV interposer have enabled wafer level system-in-package, during which multiple dissimilar dies or systems can be integrated together. The fanout wafer level packaging balanced well the cost and performance for most high-end applications.

Dr. Richard RAO, Senior Principal Engineer at Marvell Technology

Dr. Richard RAO is currently a Senior Principal Engineer at Marvell Technology and a Senior Member of IEEE. Prior to joining Marvell, he was a Fellow of Microsemi (Microchip) Corp and a consultant engineer at Ericson Inc. His responsibilities include the development of design for reliability flows for advanced circuits, packaging, and chip to package interaction. He was the chair of IEEE EPS (Electronics Packaging Society) Reliability Technical Committee and co-chairing the reliability roadmap for the IEEE Heterogenous Integration Roadmap. He is also the general chair and technical program chair for the IEEE REPP (Reliability of Electronics and Photonics Packaging) Symposium. He also serves as the technical committee chairs for the IEEE IRPS (International Reliability Physics Symposium). He has given many invited talks and keynote speeches to various international conferences. He has a Ph.D. degree in solid mechanics of materials from the University of Science and Technology of China and a post-doctor research fellow at Northwestern University studying the reliability failure mechanism of advanced integrated circuits. Prior to joining Marvell, Dr. Rao held senior technical positions in reliability physics and engineering for both academia and industries. He was an assistant/associate professor at University of Science and Technology of China and a research fellow for National Science and Technology Board of Singapore.



Prof. Guoping ZHANG, Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences

Prof. Guoping ZHANG received the Ph.D. degrees in applied chemistry from Hunan University, Changsha, China, in 2010, and went to the National Packaging Research Center (PRC) of Georgia Institute of Technology in 2014 for visiting scholar research. Prof. Zhang has been with the Shenzhen Institute of Advanced Technology (SIAT), Chinese Academy of Science (CAS), Shenzhen, China, since 2011. He is now the deputy director of Institute of Advanced Materials Science and Engineering, SIAT and the deputy director of Shenzhen Institute of Advanced Electronic Materials, SIEM. He has been a senior member of IEEE Society since 2023. He is mainly engaged in the research and application of advanced packaging materials for integrated circuits. He has undertaken and participated in more than 10 projects of National Natural Science Foundation of China, National Key R&D Program, Guangdong Provincial Science and Technology Innovation Team, Guangdong Provincial Key R&D Program, Shenzhen Science and Technology Program, and enterprise transversal, etc. He has published more than 100 SCI and EI papers, applied for more than 60 patents, obtained 20 authorized patents, 2 international PCT patents, and realized 5 patent transfers. In the transformation of scientific research achievements, he realized the transfer and transformation of patented technology and incubated the establishment of a high-end electronic packaging materials company.

Speech Description:

As Moore's Law slows down, it is imperative to accelerate the deployment of advanced packaging technologies to meet the needs of high-end chips in terms of integration, multi-function, and low cost. Shenzhen Institute of Advanced Electronic Materials is committed to the core technology breakthrough and technological innovation leadership of advanced electronic materials and aims to build an internationally leading and 'irreplaceable' platform. With more than 10 years of R&D investment and technology accumulation, it can provide system solutions in key materials for advanced packaging of integrated circuits. In particular, the developed high-temperature-resistant temporary bonding materials by the research team have been widely used in advanced packaging fields such as wafer-level packaging, 2.5/3D packaging, and heterogeneous integration. This speech mainly introduces the high temperature resistant temporary bonding/debonding material (WLP TB5160/WLP LB601) recently developed by our research team. The material has the advantages of excellent corrosion resistance, temperature resistance up to 400 °C, meeting the high productivity requirements of room temperature bonding, and compatibility with laser/mechanical debonding methods, and is suitable for high-temperature and high-stress applications in the semiconductor industry.

Dr. Ning DA, Sr. Operations Manager and Semiconductor Opportunity Leader in China SCHOTT Glass Technologies (Suzhou) Co., Ltd.

Dr. Ning DA graduated from the University of Erlangen-Nuremberg, Germany. He has nearly 20 years' experience in the field of glass, glass ceramics and other brittle materials. He joined Schott Glass in 2013 and has been deeply involved in the technology research & development, and application of glass materials in the fields of consumer electronics and semiconductor industries. Currently, he is mainly responsible for the production and operation of SCHOTT glass wafers and related semiconductor technology products, as well as the promotion and application in the Chinese market. He has published more than 30 academic papers and applied for more than 10 PCT patents on glass materials and their applications.

Speech Description:

SCHOTT is a multinational high-tech company specializing in the field of special glass and glass-ceramics. With more than 130 years of material accumulation and technology development, we provide a wide range of high-quality products and solutions and assist customers in many industries to achieve incessant success. SCHOTT is an innovation driver in many industries, such as semiconductor, medicine, household appliances, consumer electronics, optics, life sciences automotive and aviation. Especially, the glasses provided by SCHOTT are widely used in the fields of 3D imaging and sensing, MEMS, and wafer level packaging, etc.

In the more than Moore era, with the development of the chiplet technology, the integrated circuit industry has put forward higher and higher requirements for chip types, quantities, high density, and integration. As an ancient material, glass is gradually favored by chiplet technologies for its excellent optical properties, stable chemical & thermal resistance, and customizable expansion coefficient & thickness. SCHOTT is continuously developing glass materials with various properties according to the needs of the global market, and fabricating glass wafers, carrier plates, or TGV of required specifications to meet the needs of current integrated circuit development. This speech mainly introduces that SCHOTT can offer large-scale mass-produced glass wafers and substrate materials with a wide range of thickness from 0.03 to 20mm or above. In addition, warpage, thickness tolerance, and TTV are all strictly controlled. Depending on the application, the glass wafers could be offered with various coefficient of thermal expansion (CTE) range from 3.2x10-6 to 9.4x10-6/^{o}C upon request. The speech also makes an in-depth explanation of the properties and performance of glass materials that affect the chiplet processes, so as to assist the development of chiplet industry.

Mr. Zheng HAN, Senior Manager of JSR Electronic Materials (Shanghai) Co., Ltd.

Mr. Zheng HAN, he is a Sales Department Senior Manager in JSR Shanghai company. His current interest is to contribute to next generation advanced packaging for WLP/PLP and PCB industry. Today, he will present development status and roadmap of plating photoresist and photo-imageable dielectrics for advanced packaging. Furthermore, he will also introduce novel low Df polymer for PCB industry.

Speech Description:

As advanced packaging technologies evolve, the importance of the redistribution layer (RDL) is growing. The RDL in an advanced packaging works not only for making bond pad location or expanding the interconnection area beyond die size, but also for connecting between dies with high density. Moreover, an advanced packaging requires a tall copper bump for making package on package (PoP) structure. We developed novel plating photoresists and dielectric materials for RDL and PoP that an advanced packaging requires. The photoresist (PR) shows excellent chemical resistance, good coating performance and great lithographic performance with high aspect ratio on sputtered copper. And our photo-imageable dielectric (PID) showed low residual stress, low shrinkage, low dielectric loss and great lithographic performance. Furthermore, we have been developing novel low Df polymer for PCB industry in order to further contribute to the ever-evolving advanced packaging technology.

Dr. Ziyu LIU, Fudan University

Dr. Ziyu LIU is a faculty member at the School of Microelectronics, Fudan University, and also serves as a supervisor for master's students. She completed her postdoctoral fellowship in the Department of Electronic Engineering at the City University of Hong Kong, China. With 11 years of experience in the field of advanced packaging and 3D integration, Professor Liu's primary research focuses on advanced packaging technologies, including 2.5D/3D integration, wafer-level packaging, and system-level packaging. Her research involves design, modeling, process development, as well as mechanical, thermal, and electrical simulations. Notably, she has made innovative explorations in high-density interconnect bonding techniques, silicon through-hole technology, 3D passive device processes, models, and simulations. Professor Liu has published more than 50 academic papers in top packaging conferences, and has applied for and obtained 22 patents related to packaging. Additionally, she maintains cooperative relationships with several well-known domestic packaging enterprises, including Huawei, Tongfu, and Huajin Semiconductor.

Dr. Qian WANG, Tsinghua University

Qian WANG received Ph.D in 2001 from Tsinghua University, China. Then started postdoctoral work at RCAST (Research Center for Advanced Science & Technology), the University of Tokyo and NIMS (National Institute for Materials Science) in Japan until 2003. From 2003.8, he joined Samsung and worked in SAIT (Samsung Advanced Institute of Technology) as a senior engineer. From 2006 to 2009, he went back to mainland China and worked in Samsung SSCR as a principal engineer and leader of Technology Development Group. Since 2010.3, he joined Institute of Microelectronics, Tsinghua University as an Associate Professor, his research focus on advanced packaging technologies such as SiP, MEMS Packaging, WLP, 3D integration, chiplet integration and Heterogeneous Integration etc., Packaging reliability and failure analysis.

Speech Description:

Hybrid bonding has been regarded as a critical ultra-high-density interconnect technology for Chiplet integration and data-intensive applications, such as data center, high-performance computing (HPC) and artificial intelligence (AI). In general, hybrid bonding can be realized by means of chip to chip (C2C), wafer to wafer (W2W) and chip to wafer (C2W) hybrid bonding. Considering of the throughout issue, C2C hybrid bonding will not be applied in high-volume manufacturing. Meanwhile, W2W hybrid bonding is limited because of the similar chip size and yield issues. C2W hybrid bonding can provide the flexibility for assembling variable chip sizes, thus it is suitable for chiplet integration and will be the mainstream. However, C2W hybrid bonding does introduce process complexity and face challenges such as particles and contaminants due to singulation, requirement of higher accuracy picking & placement, topography control of the Cu/dielectric surface, CMP process for metal recess and flat surface. Owing to the above rigorous process requirements, C2W hybrid bonding features a narrow process window and has a low bonding throughout.

Dr. Li GONG, General Manager of Suss MicroTec (Shanghai) LTD

Dr. Li GONG has studied material sciences at the university Erlangen-Nuernberg Germany. He has joint Fraunhofer Institute for Integrated Circiuts in Erlangen in 1987. His main research fields were semiconductor process technologies and measurement techniques. He has published over 20 scientific papers in magazines and international conferences. He has received the Ph.D from the university Erlangen-Nuernberg. After many years teaching and research work, he joint Suss MicroTec in 1994. Since 2001 he is the general manager of Suss MicroTec (Shanghai) LTD. Dr. Gong is experienced in the field of semiconductor processes and equipment.

Mr. Yun CHEN, Sales manager of ACM Research (Shanghai), Inc.

Mr. Yun CHEN, with a bachelor's degree, worked in CR Micro from 2014 to 2018. He was responsible for the debugging and optimization of front-end Track process. Since he joined ACM Shanghai in 2018, he has been responsible for the research and development and debugging of advanced packaging wet process tools, advanced packaging wet process and electroplating tools technical sales, etc., and is currently in charge of advanced packaging and third-generation semiconductor sales at ACM Shanghai. He has more than 8 years of semiconductor process and technical sales experience in the field of front-end process and advanced packaging.

Speech Description:

With the ever-increasing chip stacking density and the demand for multi-chip integration, HDFO, 2.5D/3D and other more advanced wafer-level packaging technologies have been launched in China, and the requirements for related tools have continued to increase. ACM Shanghai has successfully solved the problems of warpage wafer handling and process, and successfully developed advanced single electroplating technologies/patents such as high-speed electroplating, special motion control stirring paddles, and six-element alloy elastic contacts. The electroplating deposition rate is well controlled at the same time as the electroplating uniformity, silver content and other parameters, effectively helping customers to increase production capacity while ensuring quality. In addition, ACM Shanghai also provides a complete set of advanced packaging wet-process solutions such as coating, developing, PR stripping, etching and cleaning.

Dr. Haibo FAN, Senior Principal Engineer of Nexperia Hong Kong, China

Dr. Haibo FAN, working as Senior Principal Engineer in Packaging R&D-Advanced Material Technology and Modeling, Nexperia Hong Kong, China. He got his PhD degree from Hong Kong University of Science and Technology (HKUST), China, then worked in HKUST, Philips LED lighting global R&D Center, NXP Hong Kong, China and Nexperia Hong Kong, China with 20+ year experience on simulation, and 15-year industry experience on design and reliability; He authored or co-authored more than 50 peer-reviewed technique publications, published 2 books and 3 book chapters.

Speech Description:

Simulation Driven Product Design and Development for Robust Power Package

In this talk, challenge in design and reliability from die level to board level will be discussed and several cases are demonstrated to show how designs are driven by simulation to achieve robust power package designs. Application of simulation AI-enabled simulation on semiconductor process and reliability will be discussed based on a methodology with a combination of machine learning and finite element analysis (FEA) as well.

Dr. Jing ZHANG, Head of Shanghai Innovation Center, Heraeus Electronics China

Dr. Jing ZHANG, head of Shanghai Innovation Center, Heraeus Electronics China, graduated from Delft University of Technology. His research of interests includes power electronic packaging material, process, and reliability. In 2017, he joined Heraeus, focusing on advanced packaging and reliability evaluation for the WBG semiconductor devices. Dr. Zhang has led or participated in more than 30 domestic and international R&D projects. Results of these projects have been transferred to many industries including new energy vehicles, high-speed rail, and semiconductor lighting. He has published 20 papers, authored 1 book chapter, and presented 9 reports as invited speaker at international academic conferences. Dr. Zhang is the Founding Chairman of IEEE Electronics Packaging Society (EPS) Benelux Branch, the Executive Secretary of the International Technology Roadmap for Wide Bandgap Power Semiconductors (ITRW), and a member of the Packaging Working Group. He also serves as a member of the Technical Committee of the Center for Shanghai Silicon Carbide POWER Devices Engineering & Technology Research, a member of the Youth Committee of the China Advanced Semiconductor Industry Innovation Alliance, a member of the Packaging Branch of the China Third Generation Semiconductor Roadmap Committee, and a member of the Nanotechnology Sintered Material Standardization Committee. He is an off-campus supervisor of master's students at Fudan University.

Speech Description:

Die Top System–A revolutionary solution for packaging and interconnection of SiC devices. As SiC power devices are increasingly used in many applications to enable higher power densities and switching frequencies, it becomes vital important to develop suitable packaging materials and solutions to maximize the benefit of such devices. One of the critical packaging processes is the interconnection of the upper die surface. However, traditional aluminum bonding wires are reaching their limits in terms of current carrying capability, thermal conductivity, and reliability for SiC modules. Fortunately, copper wire bonding based on Heraeus Die Top System (DTS) creates robust interconnections and provides higher current capability and reliability. In this presentation, the DTS technology will be explored in detail to show how and to what extent the solution can maximize the thermal, electrical performance and reliability of WBG devices.

Prof. Chuantong CHEN, Osaka University

Prof. Chuantong CHEN, received the master's degree and Ph.D. degree in mechanical engineering from Nagoya Institute of Technology, Japan, in 2012 and 2015, separately. From 2016 to 2019, he was an assistant professor at Institute Scientific and Industrial Research, Osaka University, Japan. He became to an associate professor in Osaka University from 2020. His research interest includes lead-free soldering, Ag sinter joining, Nano-joining, 3D packaging, and power electronics packaging. Prof. Chen was a recipient of some awards and honors including the IEEE ICEP Outstanding Technical paper Award in 2023, and the IEEE CPMT Japan Chapter Young in 2019. He has published including IEEE T Power Electr, Acta Mater, Scripta Mater, Appl Phys Lett, more than 100 journal papers and about 70 conference papers in above fields. He also applied and obtained 15 Japanese and international patents, including 3 US patents. Prof. Chen serves as technology committee member of IEEE ICEPT from 2020, and serves as the committee member of Kansai branch of the Japanese Electronics Packaging Society from 2020, and also a committee member of International standardization for the third-generation semiconductor packaging substrate material, interconnections, heat conduction evaluation system and equipment in Japan from 2018.

Speech Description:

SiC and GaN have a wider band gap than Si, and they are able to withstand both high-temperature and high-frequency operation. The SiC and GaN can reduce power loss and overall downsize the power electrical equipment. Operation temperature of SiC power modules may achieve above 250℃ due to higher power application. Silver (Ag) sinter joining is becoming an important interconnection technology for die attach in power electronics. It exhibits superior process ability, high-temperature resistance and long-time durability to traditional connection methods such as solder joining or conductive adhesive joining. Massive works have demonstrated Ag sinter paste is capable to achieve a robust and reliable die attach on DBC substrate under a mild sintering condition (pressure-less, low temperature and atmospheric sintering). However, Ag sinter joining is also facing some huge issues. In this presentation, we will summary the Ag sinter joining and propose some new die attach technologies to achieve for the low material cost and high reliability in high temperature of SiC power modules.

Prof. Bin WANG, Tsinghua University

Prof. Bin WANG, he is associate professor of the Department of Electrical Engineering of Tsinghua University, doctoral supervisor, IET Fellow, distinguished professor of oasis scholars of Shihezi University, deputy director of Beijing International Science and Technology Cooperation Center for Green Energy and Power Security, and vice chairman and secretary-general of IEEE China Satellite Substation Committee. He has been engaged in teaching and research in the fields of fault analysis and safety defense for AC/DC hybrid power grids, as well as health diagnosis and causal analysis for power grids based on artificial intelligence. He completed 18 key projects such as the China Association for Science and Technology International Science and Technology Organization Affairs Special Project and the Natural Science Foundation of China as PI, and won the second prize of the 2017 National Technology Invention Award and 8 provincial and ministerial level first prizes in Beijing City, Shaanxi Prov., Jilin Prov., Fujian Prov., and China Electric Power Science and Technology Awards.

Speech Description:
Introduce the security requirements and technical challenges of the AC/DC hybrid power grid carrying a high proportion of renewable power generation. From the two levels of transmission network and distribution network, the relevant key technologies such as fault analysis, fault detection, relay protection, fault location, Artificial Intelligence for IT Operations are introduced.

Prof. Yunhui MEI, Tiangong University

Yunhui MEI, Professor, Executive Vice President of School of Electrical Engineering, Tiangong University. He has been engaged in the research of power electronic device packaging and reliability for a long time. In recent years, he has presided nearly 30 projects. He is serving as a director of the China Power Supply Society, deputy director of the Component Committee, IEEE Senior Member, editorial board member of the Journal of Power Supply, and deputy chairman of the Tianjin Power Supply Society. He has published over 140 academic papers, including 97 SCI papers and 27 granted invention patents. I have won the IEEE CPMT Young Award, the First Prize of the Technology Invention Award of the China Power Supply Society, the First Prize of the Technology Invention Award of the China Electrical Engineering Society, and the First Prize of the Tianjin Technology Invention Award, Henry Fok Education Fund of the Ministry of Education, Science and Technology Award for Youth in Colleges and Universities, IEEE International Power Electronics Annual Conference APEC Best Presentation Award, National Third Generation Semiconductor industry Technology Innovation Strategic Alliance (CASA) 'Special Contribution Award', etc.

Scott CHEN, SVP of Central Development Engineering in ASE (Advanced Semiconductor Engineering)

Scott CHEN received B.S. degree in Chemical Engineering from NTU (National Taiwan University, China). And Master degree of Executive MBA Program from NTU. He has been worked on each of assy technology, MEMS/sensor, bumping, flip chip, advance package technology and SIP solution over 30 yrs.
Scott started worked for Texas Instruments Taiwan Ltd., China and Motorola Taiwan Motorola Electronics Taiwan Ltd., China for 10 yrs. In the recent 20 yrs of fast growing in semiconductor technology, He has not only been leading R&D team in new, variety and advanced assembly technology in ASE, but also promote the technology and business to customers. He has been vice chairman of Semi Taiwan MEMS committee (China) in 2013-14 and also been Speaker or Panelist Speaker in many Semicon workshop, ex. Semicon Taiwan (China), Semicon West, Semicon Japan, ECTC, and IMPACT.

Dr. Weisu CHEN, Deputy General Manager of Quantech (Guangzhou) New Materials Co., LTD.

Dr. Weisu CHEN worked as an equipment engineer in Taiwan Industrial Technology Research Institute (China) from 1997/10/1 to 2002/10/1. 2002/11/1-2003/10/1 Served as Technical Manager of Taiwan RiTDisplay Technology Co., LTD., China. 2003/11/1-2017/10/1 Served as Supervisor and Manager of R&D Department of Taiwan Industrial Technology Research Institute (China). 2017/11/1-2019/10/1 Worked in PSK Co., LTD. (Korea). 2019/11/1-2020/10/1 Served as a Chair Professor in the Railway Power Supply and Electrical Department of Shandong Polytechnic College. 2020/10/1 Served as Deputy General Manager of Quantech (Guangzhou) New Materials Co., LTD. in Guangzhou headquarters of the company, responsible for the establishment of high-end electronic spin-coating chemical material class 10&100 clean room factory and the project development of mass production products.

Speech Description:
The high reflectance insulating layer protective film used in semiconductor or display optical devices is made of Bragg Reflection structures formed by repeated overlapping coating of high index metal-containing and low index silicon-containing insulating layers. In this paper, the manufacturing process, baking process, optimization of surfactant formulation of ultralow refractive index Spin-on Glass (SOG) encapsulation insulating layer material, the effect of aging in air on coating defects, and the effect of filtering SOG solution for fine dust on film surface are reported. The minimum refractive index (n) of SOG reported in this paper can

be lower than 1.2@633nm wavelength, and the optimum baking process is three steps of low, middle and high temperature baking 80℃/150℃/300℃, respectively. The optimal material weight ratio of surfactant is 1 basic unit. Isolation of water and/or oxygen in the air can eliminate spin coating defects. The fine dust on the film surface is eliminated after filtrating the liquid. At present, the SPC data of this material has reached the mass production specification.

Dr. Wenbiao RUAN, R&D director of Xiamen Sky Semiconductor Technology Co. Ltd.

Dr. Wenbiao RUAN, majoring in Electronics and Solid-State Electronics at the Chinese Academy of Sciences, currently serving as the Director of R&D at Xiamen Yuntian Semiconductor Technology Co., Ltd., responsible for the research and development of processes such as through glass via (TGV), fanout packaging (WL-FO), wafer level packaging technology, and glass based high-frequency devices. He has successively served in SMIC., Institute of Microelectronics and Detection Technology. In 2010, he was appointed as an associate researcher at the Institute of Microelectronics, conducting research on the modeling of integrated circuit manufacturing processes and manufacturability design methodology for 65 nm and below node, and participating in and completing multiple national major special research projects. Published over 10 articles and applied for 18 patents.

Speech Description:

IPD (Integrated Passive Devices), which applies mature and advanced integrated circuit manufacturing processes, has the following advantages compared to traditional passive devices: significantly reduced volume, lighter weight, higher performance, and better consistency, making it an effective solution for miniaturization and high integration requirements of RF systems. Based on glass substrates, Yuntian has successfully developed TGV manufacturing technology, reaching international advanced levels. It has researched high aspect ratio TGV filling technology and the ability to design and implement multi-layer RDL wiring. On this basis, it has closely cooperated and collaborated with IPD design enterprises to develop high-performance passive components such as inductors, capacitors, filters, millimeter wave antennas, etc., laying the technical foundation for achieving high-density and miniaturized high-frequency integrated systems.

Prof. Hongjun JI, Harbin Institute of Technology, Shenzhen

Prof. Hongjun JI, studied at Harbin Institute of Technology from 1999 to 2008, received his Ph.D. in engineering and is currently a professor in the School of Materials Science and Engineering at Harbin Institute of Technology (Shenzhen). He has long been engaged in the basic and applied basic research of power ultrasound in the fields of micro-nano joining and advanced interconnection in electronic packaging. His main research interests include ultrasonic processing principles and technologies (ultrasonic assisted synthesis of materials, ultrasonic metal welding, ultrasonic assisted plastic deformation, and microstructure and properties evolution under ultrasonic excitation, etc.), and advanced electronic packaging interconnect materials and micro-nano joining technologies (wire bonding, and chip bonding, etc.). More than 70 SCI papers have been published in international high-level professional journals, such as Scripta Materialia, Ultrasonics Sonochemistry, and more than 50 papers have been published in international conferences. Furthermore, he has been invited to deliver oral presentations at ECTC, ICEPT and other international conferences on electronic packaging more than 40 times.

Speech Description:

Chip interconnection with low process requirements, high interconnection quality, and excellent stability is preferred in advanced packages characterized by high thermal/electrical conductivity, low temperature bonding and high reliability. Low-temperature Cu-Cu bonding technology is the key technology of future advanced packaging technology. Compared with the Sn-based soldering process currently used, low-temperature Cu-Cu bonding technology provides fine pitch interconnection, excellent electrical and thermal conductivity, and better reliability. Based on the background of low-temperature chip interconnection in advanced packaging, this oral presentation will introduce the latest research progress of low-temperature Cu-Cu bonding for advanced packaging interconnection applications. Combined with the research results of our research group, the Cu-Cu ultrasonic welding process and low-temperature Cu-Cu bonding technology using nanomaterial interlayer, and low-temperature Ag-Ag bonding technology will be introduced.

ORAL SESSIONS 1&2

Friday, August 11th, 2023 10:00 ~ 11:45

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 1	Oral Session 2
Venue Room 1 **Session** Advanced Packaging **Chair** Dr. Qidong WANG	**Venue** Room 2 **Session** Packaging Materials & Processes **Chair** Prof. Xu LONG
Keynote 10:00-10:30 **Chiplets and Advanced Packaging for Future Computing and Communication** *Dr. Cheng-Tar Terry WU* Director of Samsung Electronics	**Keynote** 10:00-10:30 **High Temperature Temporary Bonding/Debonding Materials (WLP TB5160/WLP LB601)** *Prof. Guoping ZHANG* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences
23 10:30-10:45 **Technology Development of Wafer-level Ultra-high Density Fan-out (UHD FO) Package** *Dongzhi Fu* Huatian Technology (Kunshan) Electronics Co., Ltd.	21 10:30-10:45 **Reflow Soldering Using Flux-sprayed Solder Preforms** *Fred Fuliang Le* Nexperia HK
54 10:45-11:00 **A High Density QFP With Hybrid Lead** *Chao Ma* NXP semiconductor	34 10:45-11:00 **A Thin Film Metallization Process Development for Silicon Nitride Ceramic Substrates in Power Electronics Packaging** *Xin Chen* School of Materials Science&Engineering Beijing Institute of Technology
55 11:00-11:15 **Deposition Efficiency Study on Wafer Level Gold Plating based on Cyanide-free Electrolyte** *Zhaowei Jia* ACM Research (Shanghai), Inc.	35 11:00-11:15 **Preparation and performance analysis of micro-nano silver powder for solar cells** *Siwei Tang* Central South University
87 11:15-11:30 **Fan-Out Embedded Bridge Solution for Chiplet/HBM Integration** *Mark Liao* PATSD Division, SPIL	78 11:15-11:30 **The Influence of Welding Interfacial Voids on the Thermal Conductivity of Space-borne High-power Electronics** *Le Zhang* China Academy of Space Technology (Xi'an)
125 11:30-11:45 **Electrical Performance Enhancement Solution with FO-EB in HPC Application** *Po Yuan Su* Siliconware Precision Industries Co., Ltd.	

ORAL SESSIONS 3&4

Friday, August 11th, 2023 10:00 ~ 11:45

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 3		Oral Session 4	
Venue	**Room 3**	**Venue**	**Room 4**
Session	**Packaging Design & Modeling**	**Session**	**Interconnection Technologies**
Chair	**Prof. Daoguo YANG**	**Chair**	**Prof. Chenxi WANG**
Keynote	10:00-10:30	**Keynote**	10:00-10:30
Electro-thermal-Stress Collaborative Simulation Optimization for Key Technologies of 3D Integration *Dr. Ziyu LIU* Fudan University		**A New Strategy of Cu/SiO2 Hybrid Bonding for Chiplet Integration** *Dr. Qian WANG* Tsinghua University	
22	10:30-10:45	119	10:30-10:45
On-Die Power-Rails Isolation Using Package Loop Inductance *Vinod Arjun Huddar* Rambus		**Enabling Low-k Liner in Ultra-high Aspect Ratio TSVs by the Timing of Vacuum Treatment in the Vacuum-assisted Spin-coating Technique** Ziyue Zhang BIT Chongqing Institute of Microelectronics and Microsystems; School of Integrated Circuits and Electronics, BIT	
24	10:45-11:00	149	10:45-11:00
Achieving non-underfill SMT process for large size packages by creative package pin map and PCB pad designs *Hongbin Shi* Huawei Technologies Co., Ltd.		**Effect of insulating material and structure on the reliability of silicon through hole under thermal stress** *Zongyang Li* Beijing Microelectronics Technology Institute	
28	11:00-11:15	189	11:00-11:15
Underfill Flow Numerical Simulation for Achieving Board Level Low Cost and High Reliability of Mobile Devices *Yiming Jiang* Huawei Technologies Co., Ltd.		**Selective Wet Etching Technology in 3D NAND Flash Manufacture** *Zihan Zhou* School of Materials Science and Engineering, Shanghai Jiao Tong University	
42	11:15-11:30	190	11:15-11:30
Rough Interface Effect on High-Temperature Reliability of TSV for Electronic Packaging *Weishan Lv* Huazhong University of Science and Technology		**Anti-oxidation property of nanotwinned copper micro-cone array for low-temperature bonding** *Peixin Chen* Shanghai Jiao Tong University	
45	11:30-11:45	200	11:30-11:45
Modeling Methodology for Mechanical Shock Reliability Enhancement Designs of Ultra-Large BGA Packages *Jianghai Gu* CISCO		**Study on Low-Temperature Bonding and Reliability of Nano-Twin Copper Micro-Cone Array** *Chongyang Li* Shanghai Jiao Tong University	

ORAL SESSION 5

Friday, August 11th, 2023 10:00 ~ 11:45

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 5

Venue **Room 5**

Session **Quality & Reliability**

Chair **Dr. Bin XIE**

46	10:00-10:15
Study on the Application of Auger Electron Spectroscopy in RDL Failure Analysis	
Yanfei Zhao	
Wintech-Nano (Suzhou) Co., Ltd.	
70	10:15-10:30
Three-point Bending Test Method Experimental Study for Package Strength and Crack Prediction through Finite Element Analysis	
Minyan Wu	
Packaging Technology Development Team, Samsung Semiconductor (China)R&D CO., LTD.	
91	10:30-10:45
Thermal fatigue behavior of Cu/Co-P/Sn/Co-P/Cu solder joint interface with crystalline/amorphous Co-P coating	
Shuang Liu	
Beijing University of Technology	
104	10:45-11:00
Study of the s hear strength behavior in flip chip under thermo mechano electrical coupling and different s older height	
Bin Zhou	
Key Laboratory for Microsystems and Microstructure Manufacturing; Harbin Institute of Technology	
185	11:00-11:15
Quantitative analysis of the interface strength of ultra-thin dielectric films based on fan-out packaging	
Zhanxing Sun	
Institute of Microelectronics of Chinese Academy of Sciences	
198	11:15-11:30
Effects of Porosity on Thermal Resistance Aging at Submicron Silver Interfaces	
Jian Wang	
School of Energy and Power Engineering, Shandong University	
210	11:30-11:45
Studies and Application of A Novel Failure Localization Method for 3D Stacked IC Chips	
Zhang Linhua	
Wintech-Nano (Suzhou) Co., Ltd.	

ORAL SESSIONS 6&7

Friday, August 11th, 2023 10:00 ~ 11:45

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 6	Oral Session 7
Venue Room 6	**Venue** Room 7
Session Optoelectronics and New Display & MEMS Packaging	**Session** Power Electronics & The new energy and new power system
Chair Prof. Jianhua ZHANG	**Chair** Prof. Huaiyu YE
Keynote 10:00-10:30 **Development of high reflectance insulating film materials for packaging semiconductor optical devices** *Dr. WeiSu CHEN* Deputy General Manager of Quantech (Guangzhou) New Materials Co., LTD.	**Keynote** 10:00-10:30 **Robust Power Package Design with Simulation Driven Product Development** *Dr. Haibo FAN* Senior Principal Engineer of Nexperia Hong Kong, China
138 10:30-10:45 **In-plane heat transfer enhancement of phosphor layer in transmissive laser-excited white lighting** *Weixian Zhao* Huazhong University of Science and Technology	247 10:30-10:45 **Numerical simulation of bonding wire lift-off of IGBT under power cycling** *Shengjun Zhao* Faculty of Materials and Manufacturing, Beijing University of Technology
151 10:45-11:00 **Phosphor-in-glass film on AlN substrate for high-luminance white laser Lighting** *Zikang Yu* School of Aerospace Engineering, Huazhong University of Science and Technology	387 10:45-11:00 **A gate driver circuit for crosstalk suppression of SiC MOSFET in half-bridge configuration** *Longnv Li* Tiangong University
179 11:00-11:15 **A novel circular position sensitive detector (CPSD) for continuously high-precision rotary angle measurement** *Xiangxu Meng* Institute of Microelectronics of Chinese Academy of Sciences	624 11:00-11:15 **Inductor Design for Four-switch Boost/drop Power Supply Module** *Yiying Bao* Microsystem Packaging Research Center, Institute of Microelectronic of Chinese Academy of Sciences
279 11:15-11:30 **Simulation Study on Temperature Field of Packaged High Power GaN Laser Diodes** *Hui Liao* University of Shihezi	**Keynote** 11:15-11:45 **Innovative Packaging Solution for SiC Power Device** *Dr. Jing ZHANG* Head of Shanghai Innovation Center, Heraeus Electronics China
403 11:30-11:45 **The structural optimization of heterogeneous integration system in display based on thermal reliability analysis** *Sixin Huang* Huawei Technologies Co., Ltd.	

ORAL SESSIONS 8&9

Friday, August 11th, 2023 12:15 ~ 14:00

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 8		Oral Session 9	
Venue	**Room 1**	**Venue**	**Room 2**
Session	**Advanced Packaging**	**Session**	**Packaging Materials & Processes**
Chair	**Prof. Shenglin MA**	**Chair**	**Prof. Zhiquan LIU**
Keynote	12:15-12:45	**Keynote**	12:15-12:45
Embedded Silicon based Fan-out package with 2μm/2μm Line/Space multi-layer RDL *Prof. Wei WANG* Peking University		**SCHOTT Glass Wafers and Circuit Boards-Enabling Advanced Packaging of Integrated Circuit** *Dr. Ning DA* Sr. Operations Manager and Semiconductor Opportunity Leader in China SCHOTT Glass Technologies (Suzhou) Co., Ltd.	
216	12:45-13:00	97	12:45-13:00
FOStrip® Technique for Low-Cost Fan-Out Package *I-Hung Lin* Kore Semiconductor Co., Ltd.		**Selective Laser-induced Etching of Borosilicate Glass in Hydrofluoric Acid** *Yue Zhan* School of Microelectronics, Southeast University, Wuxi	
260	13:00-13:15	113	13:00-13:15
Solution to Optimize Warpage performance for 2.5D Fanout Packaging *Yue Jiang* State Key Laboratory of Mobile Network and Mobile Multimedia Technology, ZTE Corporation		**High energy dissipation composite elastomer for application as a thermal interface material through solvent-induced dis-entanglement** *Weijian Wu* Shenzhen Institute of Advanced Electronic Materials	
282	13:15-13:30	130	13:15-13:30
Influence of defects in temporary bonding pairs on the effectiveness of UV laser debonding *Jieyuan Zhang* Shenzhen Institute of Advanced Electronic Materials		**Effects of silver paste glass additive composition on co-firing behavior of a silver conductor LTCC package** *Zhuofeng Liu* National University of Defense Technology	
360	13:30-13:45	133	13:30-13:45
Study on Low Temperature Interconnected nt-Cu/In Solder Joint Interface in System in Package *Zicheng Sa* Harbin Institute of Technology		**Copper Low Temperature Co-fired Ceramic: next generation of LTCC for low-cost, high strength and high frequency space applications** *Shicheng Yang* China Aerospace Science and Technology Institute 504	
501	13:45-14:00	206	13:45-14:00
Thermal Performance of 2.5D Packaging with the Through Glass Via (TGV) Interposer *Jin Zhao* Beijing University of Technology		**Carbazole-grafted Polyimide with Enhanced Adhesion to Smooth Copper** *Zimeng He* Shenzhen Institute of Advanced Technology	

ORAL SESSIONS 10&11

Friday, August 11th, 2023 12:15 ~ 14:00

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 10		Oral Session 11	
Venue	**Room 3**	**Venue**	**Room 4**
Session	**Packaging Design & Modeling**	**Session**	**Interconnection Technologies**
Chair	**Dr. Xiangmeng JING**	**Chair**	**Prof. Yingxia LIU**
Keynote	12:15-12:45	202	12:15-12:30
Can SIP be the way out for China in the post-Moore era? *Prof. Zhong TIAN* University of Electronic Science and Technology of China		**Theoretical analysis and prediction for thermal stress of sintered silver interconnection structure based on modified Suhir's solution** *Jiahui Wei* Faculty of Materials and Manufacturing, Beijing University of Technology	
57	12:45-13:00	204	12:30-12:45
Radiated Emissions Prediction of an Electronic Packaging Based on Near-field Scanning *Di Wang* Zhejiang University		**Toward next generation interconnection technology: Ag/Cu sinter joining and their innovative application** *Yue Gao* Heraeus Electronics	
69	13:00-13:15	220	12:45-13:00
Prediction of Electromagnetic Leakage from Circuits inside Package *Si-Yao Tang* Zhejiang University		**Mode I fracture of graphene reinforced Sn-Ag-Cu solder joints** *Jianfeng Wang* Beijing University of Technology	
79	13:15-13:30	221	13:00-13:15
Mechanical properties of IGBT module under Temperature shock test considering residual stress *Rui Wang* NARI-GEIRI Semiconductor Co., Ltd.		**Thickness effect on shear fracture toughness of sintered silver joints** *Rong Kang* Beijing University of Technology	
94	13:30-13:45	301	13:15-13:30
The Effect of Pore Defects on the Interfacial Thermal Resistance of GaN-Diamond Heterostructure *Chao Yang* School of Energy and Power Engineering, Shandong University		**A Novel Low-temperature Co-Co Direct Bonding for Future 3D Interconnections** *Xiaoyun Qi* Harbin Institute of Technology	
117	13:45-14:00	319	13:30-13:45
Low Modulus Polyimide Coating on Wedge Bond to Improve Wire Bond Robustness in Thermal Cycling *Ou Dong* Nexperia		**Low-temperature direct bonding of strengthened glass chips for optical imaging and co-packaged Optics** *Yu Du* Harbin Institute of Technology	
		417	13:45-14:00
		A Novel Focused Induction Heating Method For The Interconnection Between High-power Devices And Integrated Circuit Board *Peng Cui* School of Materials Science and Engineering, Harbin Institute of Technology, Shenzhen	

ORAL SESSIONS 12&13

Friday, August 11th, 2023 12:15 ~ 14:00

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 12	Oral Session 13
Venue Room 5 **Session** Quality & Reliability **Chair** Prof. Xiaofeng YANG	**Venue** Room 6 **Session** MEMS Packaging & Emerging Technologies & Applications of Electronic Technology for Artificial Intelligence **Chair** Prof. Jintang SHANG
264 12:15-12:30 **Study on cracking behavior of sintering silver joints based on cohesive zone model** *Rui Yang* Beijing University of Technology	**Keynote** 12:15-12:45 **Automotive Electronic Packaging and Its Future Development** *Scott CHEN* SVP of Central Development Engineering in ASE (Advanced Semiconductor Engineering)
292 12:30-12:45 **Development of Low-warpage Bonding Pair by Finite Element Analysis** *Yalin Zeng* Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences	64 12:45-13:00 **Location Identification Method for Soldering Devices of SMT Based on ConvRes-UNet** *Yiqing Yang* Guilin University of Electronic Technology
307 12:45-13:00 **Micro Solder Defect Inspection Using Infrared Sequence and OmniScaleCNN Deep Learning Model** *Ye Jiang* School of Mechanical Science & Engineering, Huazhong University of Science and Technology	98 13:00-13:15 **Welding process expert system based on industrial internet and neural network** *Xiaochuan Xie* GuangZhou Risong Intelligent Technology Holding Co., LTD.
320 13:00-13:15 **A New High-efficient Burn-in Screening Methodology Applied in Integrated Circuits Reliability** *Yalan Sheng* SANECHIPS	122 13:15-13:30 **Structure Optimization Design of Interfacial Failure Resistance for Composite Film in Flexible Electronics** *Hongshi Ruan* College of Mechanical Engineering, Zhejiang University of Technology
326 13:15-13:30 **Failure Analysis for IIH leakage on 7nm FinFET Technology Chip** *Shuanshe Chao* State Key Laboratory of Mobile Network and Mobile Multimedia Technology	134 13:30-13:45 **Conjugated Small Molecule Crystals as A Coupling Layer Between Carbon-based Thermal Interface Materials and Heat Sink** *Daoqing Liu* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology
386 13:30-13:45 **Time Dependent Dielectric Breakdown of 4H-SiC MOSFETs in CMOS technology** *Yaqian Zhang* Delft university of technology	146 13:45-14:00 **High-Performance Thermal Interface Material with A Radial Filler Skeleton** *Jingjing Zhang* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology
420 13:45-14:00 **The prediction of the solder ball crack based on artificial neural network using S parameters** *Huanpeng Wang* Yangtze Delta Region Institute (Huzhou), University of Electronic Science and Technology of China	

ORAL SESSION 14

Friday, August 11th, 2023 12:15 ~ 14:00

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 14

Venue **Room 7**

Session **Power Electronics & The new energy and new power system**

Chair **Prof. Hongwei LIANG**

Keynote 12:15-12:45

Ag sinter joining and beyond Ag sinter joining technologies for WEB power device in high temperature applications

Prof. Chuantong CHEN

Osaka University

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323 12:45-13:00

A resonance suppression strategy of LCL-type grid-connected inverter based on compound voltage feedforward

Haichao Yan

College of Mechanical and Electrical Engineering, Shihezi University

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553 13:00-13:15

Collaborative Optimization of Multi-energy Complementary System via Game Theory

Tongqing Song

Shanghai Jiao Tong University

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621 13:15-13:30

Design Hydro-Solar-Wind Multi-energy Complementary System via Multi-Objective Optimization

Haotian Tang

Shanghai Jiao Tong University

Keynote 13:30-14:00

Fault detection and protection technology for AC/DC hybrid power grid with high proportion of renewable power generation

Prof. Bin WANG

Tsinghua University

ORAL SESSIONS 15&16

Friday, August 11th, 2023 15:30 ~ 17:45

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 15	Oral Session 16
Venue Room 1 **Session** Advanced Packaging & Advanced Manufacturing & Packaging Equipment **Chair** Prof. Wei WANG	**Venue** Room 2 **Session** Packaging Materials & Processes **Chair** Prof. Yunwen WU
Keynote 15:30-16:00 **Thermofisher solution for 3D packaging R&D and Failure analysis** *Ms. Linling CAI* Business Development Manager Thermo Fisher Scientific	**Keynote** 15:30-16:00 **Key Lithographic Materials Enabling High Density and Low-Loss Advanced** *Mr. Zheng HAN* Senior Manager of JSR Electronic Materials (Shanghai) Co., Ltd.
Keynote 16:00-16:30 **Development of Heterogeneous Integration Packaging Technology** *Dr. Daping YAO* Chairman & CEO of Jiangsu CAS Microelectronics Integration Technology Co., Ltd.	234 16:00-16:15 **Copper nanoparticle pastes with organic compounds as anti-oxidative additive for Cu–Cu bonding in air** *Xiaocun Wang* Fudan University
Keynote 16:30-17:00 **Advanced packaging tool technology and upgrading plan** *Mr. Yun CHEN* Sales manager of ACM Research (Shanghai), Inc.	241 16:15-16:30 **Suppression of Kirkendall Voids at the Interfaces of Sn/nc-Cu Solder Joints** *Xinwei Tian* School of Materials Science and Engineering, Dalian University of Technology
513 17:00-17:15 **Effect of dimension and defects on the flexibility of ultra-thin chips for wearable electronics** *Yan Pan* Shenzhen Institute of Advanced Electronic Materials,SIAT, CAS	246 16:30-16:45 **Microstructure and properties of Sn3.0Ag0.5Cu micro-bumps with nickel-coated graphite and nickel-coated carbon fibers additions** *Yihui Du* Beijing University of Technology
604 17:15-17:30 **Prediction of bonding strength for sintered Ag/DBA joints based on cohesive zone model** *Libo Zhao* Faculty of Materials and Manufacturing, Beijing University of Technology	263 16:45-17:00 **Enhancing properties of low-temperature pressureless Ag sinter-joining by optimizing solvents and hybrid particles** *Yitian Li* School of Mechanical Engineering, Jiangnan University
147 17:30-17:45 **Ablation Behaviour of Photosensitive Materials in Laser Debonding Processes for Advanced Packaging** *Fangcheng Wang* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS	265 17:00-17:15 **Rapid and low temperature Cu particle sintering for power devices with mixing of MOD ink and reductive additives** *Jianbo Xin* School of Material Science and Engineering, Harbin University of Science and Technology
	277 17:15-17:30 **Surface Protecting and Particles Removing after Wafer Sawing for Die-to-wafer Hybrid Bonding** *Hao Wang* School of Microelectronics, Fudan University

327	17:30-17:45
First Principle Study of the Adsorption Behavior of 1,2,4-Triazole on Defective Copper Surface	
Pengfei Chang	
School of Materials Science and Engineering, Shanghai Jiao Tong University	

ORAL SESSION 17

Friday, August 11th, 2023 15:30 ~ 17:45

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 17

Venue **Room 3**

Session **Packaging Design & Modeling**

Chair **Prof. Tao HANG**

148 15:30-15:45	341 17:15-17:30
A crosstalk mitigation method of DDR5 in large size LGA package	**Simulation and Optimization of Large Scale Multiport Power Supply Noise for 2.5D IC**
Keqing Ouyang	*Chenxi Yang*
State Key Laboratory of Mobile Network and Mobile Multimedia Technology	Sanechips Technology Co., Ltd.
153 15:45-16:00	350 17:30-17:45
Power Noise Coupling Simulation of DDR4 For FCBGA Packaging	**Effects of dishing and annealing temperature on wafer to wafer hybrid bonding**
Zhang Jianguo	*Yu Li*
Department of Packaging and Testing, ZTE Corporation	Wuhan University
186 16:00-16:15	
Research on the electromigration failure of W interconnects under high-temperature environment	
Yong Wang	
Zhejiang University of Technology	
240 16:15-16:30	
A combined experimental and analytical study of residual strains developed in encapsulated structures	
Xiang Li	
Institute of Electronic Engineering, China Academy of Engineering Physics	
290 16:30-16:45	
Simulation and Performance Test of High Bandwidth PCB Based on Multichannel Vertical Interconnection High Frequency Connector	
Miao Wu	
Device Technology Department National Optoelectronics Innovation Center	
293 16:45-17:00	
Optimizing Hierarchical 3-D Floorplanning with simulated annealing Algorithm	
Chengyi Liao	
Microsystem Packaging Research Center, Institute of Microelectronic of Chinese Academy of Sciences	
311 17:00-17:15	
Thermal Resistance Simulation Analysis and Test Research of Wire Bond Ball Grid Array Package	
Fang Qu	
State Key Laboratory of Mobile Network and Mobile Multimedia Technology	

ORAL SESSION 18

Friday, August 11th, 2023 15:30 ~ 17:45

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 18

Venue **Room 4**

Session **Interconnection Technologies**

Chair **Dr. Ziyu LIU**

Keynote 15:30-16:00
Hybrid Bonding Technology in 3D Packaging
Dr. Li GONG
General Manager of Suss MicroTec (Shanghai) LTD

424 16:00-16:15
Effect of ultrasound-assisted Zn content on Cu/Al interconnections in high temperature solders
Jin Zhou
Chongqing University of Technology

425 16:15-16:30
Modeling and Simulation of a High Bandwidth Conical 3D Monopole Antenna for 3D IC
Yang Wang
School of Microelectronics, Fudan University

441 16:30-16:45
Low-temperature Cu/SiC heterogeneous interconnection using Sn-Ag-Ti(La) under high-frequency ultrasound
Hao Yang
Chongqing University of Technology

450 16:45-17:00
Copper electroplating of through silicon vias (TSV) using series of nitrogen-containing heterocyclic compounds
Ke-Xin Chen
Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences

451 17:00-17:15
Reliability Study of Two-Step Plasma-Activated Copper-Copper Direct Bonding in Ambient
Liangxing Hu
Nanyang Technological University

457 17:15-17:30
Electrochemical simulation of electrodeposition growth of copper in through silicon via (TSV)
Zeng-Guang Xu
Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS

463 17:30-17:45
CPU Socket Interposer Package Level and Interconnect Manufacturability Study-Part 1: Socket Contact vs. Direct-Solder–Attach Interconnection and Part 2:iNEMI 2023 Board Assembly-CPU Socket Technology Roadmap
Paul Wang
Tyan Computer (a MiTAC company)

ORAL SESSION 19

Friday, August 11th, 2023 15:30 ~ 17:45

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 19

Venue **Room 5**

Session **Quality & Reliability**

Chair **Dr. Bin XIE**

421 15:30-15:45

Optimization of packaging process in Ag sintering for ultra-reliable SiC based power electronics

Minglu Xia

Hong Kong Applied Science and Technology Research Institute, China

598 17:15-17:30

Growth behavior of IMC at the Co-P/SAC105/Co-P solder joint interface under Thermoelectric Coupling Fields

Jing Rong

Chongqing University of Technology

467 15:45-16:00

Orientation-related stress analysis of nanotwins copper in redistribution layer for wafer-level packaging

Ze-Song Wang

Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS

643 17:30-17:45

Life Prediction of Solder Interconnects under Harsh Thermal Cycling from Microstructural Degradation

Wanyu Jiang

State Key Laboratory of Advanced Welding and Joining, Harbin Institute of Technology

472 16:00-16:15

Finite Element Simulation Study of the Effects of Kirkendall Voids in IMC Layer on Interfacial Crack and Reliability of Cu–Sn Solder Joints

Ming-Sheng Luo

South China University of Technology

514 16:15-16:30

Influence of pin position on the CDM peak current based on 2.5D and 2D package

Menghua Wang

Department of Reliability Engineering, Sanechips Technology Co., Ltd.

526 16:30-16:45

Effects of Plasma Treatment on Adhesion and Flow Behavior of Underfill in 2.5D electric package

Yuanyuan Yang

Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences

528 16:45-17:00

Electrochemical Migration Mechanism of Cu@Ag Composite Preforms by Electromagnetic Compaction for Power Electronics

Ziao Li

Wuhan University of Technology

533 17:00-17:15

Correlation Analysis on Warpage and Metal Thermal Interface Materials Thermo-mechanical Reliability of Large size FCBGA

Zhuolun Wu

State Key Laboratory of Mobile Network and Mobile Multimedia Technology

ORAL SESSIONS 20&21

Friday, August 11th, 2023 15:30 ~ 17:45

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 20	Oral Session 21
Venue Room 6 **Session** Emerging Technologies & Applications of Electronic Technology for Artificial Intelligence **Chair** Dr. Daquan YU	**Venue** Room 7 **Session** Packaging Materials & Processes **Chair** Prof. Yujie LI
Keynote 15:30-16:00 **Development of Integrated Passive Devices Based on Glass Substrate and TGV Process** *Dr. Wenbiao RUAN* R&D director of Xiamen Sky Semiconductor Technology Co., Ltd.	**Keynote** 15:30-16:00 **Characterizations of 1700V Silicon Carbide Power Modules in Planar Packaging Based on Domestic Chips** *Prof. Yunhui MEI* Tiangong University
233 16:00-16:15 **Nonvolatile Memory Devices Based on Two-Dimensional WSe2/MoS2 van der Waals Heterostructure** *Sixian He* School of Materials Science and Engineering, Shanghai Jiao Tong University	482 16:00-16:15 **Flexible silver/cellulose fabric for highly efficient and broadband EMI shielding via metal-organic decomposition approach** *Si-Yuan Liao* Shenzhen Institute of Advanced Technology Chinese Academy of Sciences
274 16:15-16:30 **Moisture-responsive Biopolymer Actuators with Programmable Deformation Behavior** *Yunxia Yang* Beijing university of technology	517 16:15-16:30 **Structural Analysis of Anisotropic Conductive Film for Liquid Crystal Displays and Semiconductor Packaging Applications** *Yadong Xu* Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences
276 16:30-16:45 **On-Chip Substrate Integrated Plasmonic Waveguide Bandpass Filter for Millimeter-Wave Applications** *Tian Yu* Xiamen university, School of Electronic Science and Engineering College	536 16:30-16:45 **Fabrication of Ultra-Thin Conformal Shielding coatings on SiP modules by Inkjet Printing Technology** *Hao Wu* Shenzhen Institute of Advanced Electronic Materials/University of Science and Technology of China
284 16:45-17:00 **Interfacial Engineering of ZnO/CdS Heterostructure for Long Cycle Life Li-O2 Batteries** *Congcong Dang* School of Materials Science and Engineering, Shanghai Jiao Tong University	540 16:45-17:00 **The synthesis and Characterization of well-dispersed submicron copper particles and the research of sintering performance** *Yi Fang* School of Materials Science and Engineering, Harbin Institute of Technology (Shenzhen)
354 17:00-17:15 **Synthesis of Cobalt Doped VSe2 Nanoflake as Cathode Material for Wearable Aqueous Zinc Ion Battery** *Xinxin Wang* State Key Laboratory of Advanced Welding and Joining, Harbin Institute of Technology	544 17:00-17:15 **Optimization of Wafer-level TTV Using RIE Applied for the Extreme Wafer Thinning** *Jinzhu Li* School of Microelectronics, Fudan University

382 17:15-17:30
Vertical Hexagonal Arrangement Structure - VHAS
Akanksha Sahoo
Engineer, Micron

586 17:15-17:30
Study on Micro-silver Joint Doped with Silicon Carbide Nanowires for Power Electronics
Mu-lan Li
Sun Yat-sen University

460 17:30-17:45
Condition monitoring of SiC power module by using time-series analysis of acoustic emission during power cycling tests
Zheng Zhang
Institute of Scientific and Industrial Research (SANKEN), Osaka University

590 17:30-17:45
A digital image correlation study on the microstructure and strain behavior of electroplated nanotwinned copper as interconnection material
Zhiqiang Zhang
Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences

ORAL SESSION 22

Friday, August 11th, 2023 18:15 ~ 20:30

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 22

Venue **Room 1**

Session **Advanced Packaging &Advanced Manufacturing & Packaging Equipment**

Chair **Prof. Sheng LIU**

Keynote 18:15-18:45
Chip to Package Interaction in Heterogeneous Integration Packages
Dr. Richard RAO
Senior Principal Engineer, Marvell Technology /IEEE HIR

238 18:45-19:00
Scallop-less Nanoscale TSV with F/O Coupling Plasma Etching
Yang Wang
School of Microelectronics, Fudan University

275 19:00-19:15
High-precision positioning detection technology for large-size panel-level package chips
Zhihang Chen
School of Electromechanical Engineering, Guangdong University of Technology

324 19:15-19:30
A New Numerical Algorithm to Estimate the Average Travel Time of Workpiece in Package and Reliability Production Machines
Niuyi Sun
Sanechips Technology Corporation

435 19:30-19:45
Optimization of Laser-induced deep etching for TGV fabrication in fused silica
Jingli Liu
Southeast University

490 19:45-20:00
Research on AI-Based Gold Removal Technology for Aviation Connector Cup Cavity Surface
Zhang Yongzhong
Intelligent Electronic Manufacturing Research Center Beijing City University

ORAL SESSION 23

Friday, August 11th, 2023 18:15 ~ 20:30

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 23

Venue Room 2

Session Packaging Materials & Processes

Chair Dr. Liyin GAO

328 18:15-18:30
Investigation on Silver Nanowire/Resin-Induced Liquid Crystal Polymer Metallization
Yongjiang Zhang
Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology

329 18:30-18:45
Study on low temperature sintering mechanism and performance of multiscale silver paste
Yiping Wang
State Key Laboratory of Advanced Welding and Joining, Harbin Institute of Technology

333 18:45-19:00
Green and high-efficiency CMP Slurry for Cu planarization
Jiale Zhang
Southern University of Science and Technology

338 19:00-19:15
Preparation and characterization of submicron silver particles with the nanoscale surface structure for high-reliability packaging
Bolong Dong
School of Materials Science and Engineering, Harbin Institute of Technology (Shenzhen)

351 19:15-19:30
Influence of Bonding Conditions on Low-temperature Solid-state Bonding of Cobalt Based Nanocones
Silin Han
Shanghai Jiao Tong University

367 19:30-19:45
Analysis of Metallization Effects of Pressure-Assisted Cu Nanoparticle Sintering on DBC by Experiment and Nanoscale Simulation
Shizhen Li
Southern University of Science and Technology

388 19:45-20:00
SIP SOLDER PASTE VIA POWDER CLUSTER DESIGN HARVEST BOTH SLUMP RESISTANCE AND TEMPERATURE CYCLING RELIABILITY
Ning-Cheng Lee
ShinePure Hi-Tech

432 20:00-20:15
A Novel No-Clean Type 5 SAC305 Solder Paste Reflowed under Air Atmosphere
Jinjin Bai
Indium Corporation of Suzhou

437 20:15-20:30
The influence of pattern size on the profile and microstructure of electroplated copper pad, redistribution layer and via for advanced packaging
Jin-Hao Liu
Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences

ORAL SESSION 24

Friday, August 11th, 2023 18:15 ~ 20:30

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 24

Venue **Room 3**
Session **Packaging Design & Modeling**
Chair **Prof. Fengman LIU**

400 18:15-18:30
Die Shift Simulation in Panel Level Packaging
Bin Gu
ST Microelectronics

406 18:30-18:45
Interfacial reliability analysis and structural optimization of System-in-Package module
Sixin Huang
Huawei Technologies Co., Ltd.

408 18:45-19:00
Optimizing conformal shielding scheme with quantitative analysis
Xinyu Zhang
Microsystem Packaging Research Center, Institute of Microelectronic of Chinese Academy of Sciences

512 19:00-19:15
Research on Optimized Modeling of Package Warping Phenomenon
Lin Wu
ChangXin Memory Technologies, Inc.

585 19:15-19:30
Thermal Stress Field of Al2O3/Al-Ni Nanofoil/Ni Solder Joints by Self-propagation Reactions
Shengbo Huang
Wuhan University of Technology

626 19:30-19:45
High-Throughput Screening Modeling for Exploring Low-k Dielectric Constant Crystals
Zikang Guo
Shanghai Jiao Tong University

664 19:45-20:00
Analysis of Complex BGA Transition for Equivalent Circuit Modeling
Kangrong Li
Xi'an Microelectronics Technology Institute

684 20:00-20:15
A Lossy Filter Using Quarter-mode Substrate Integrated Waveguide and Coplanar Waveguide
Shihao Xie
Shanghai University

695 20:15-20:30
Development of Low-Loss and Low-Cost Air-Filled Transmission Lines based on Advanced Glass Wafer-Level Packaging
Jing Cai
Xiamen University

ORAL SESSION 25

Friday, August 11th, 2023 18:15 ~ 20:30

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 25

Venue **Room 4**

Session **Interconnection Technologies**

Chair **Prof. Yu ZHANG**

471 18:15-18:30
Effect of soldering temperature on the properties of Cu/SAC0307/Al joints with dual ultrasound assistance
Yongchong Ma
Chongqing University of Technology

473 18:30-18:45
An Exploratory Study to Achieve Cu Pillar Direct Bonding with Assistance of Bimodal-sized Cu Nanoparticle Paste by Low-Temperature Thermocompression Bonding in Air
Li-Ping Wang
South China University of Technology

522 18:45-19:00
Evaluation and Mechanism Study of a Novel Green Chemical Mechanical Polishing Slurry for Cobalt Interconnects
Zisheng Huang
School of Materials Science and Engineering, Shanghai Jiao Tong University

525 19:00-19:15
Modeling and Reliability Characterization of Micro-coil Springs for Ceramic Grid Array Integrated Circuits
Minghua Zhang
Beijing Spacecraft

599 19:15-19:30
Design and Fabrication of Flip-chip Interconnection for Superconducting Circuits Based on Silicon Bumps
Kun Li
Shanghai Institute of Microsystem and Information Technology

610 19:30-19:45
Wafer-level Sn-Ag-Cu/SiO2 Transient Liquid Phase Hybrid Bonding (TLP-HB) Technology
Shuai Zhang
Zhejiang Lab, ZJ Lab-Enflame Joint Innovation Research Center

660 19:45-20:00
Ultrasonic-accelerated TLPB with Ga-paste Solder for Low-temperature Electronics Interconnects
Yi Chen
Wolfson School of Mechanical and Manufacturing Engineering Loughborough University, Leicestershire, UK

669 20:00-20:15
Quantitative Microstructural Data of Bulk Solders and Joints under a New Framework of MicroStructure Hierarchy Descriptor (μSHD)
Kaiwen Zheng
Sun Yat-sen University

ORAL SESSION 26

Friday, August 11th, 2023 18:15 ~ 20:30

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 26

Venue **Room 5**

Session **Quality & Reliability & Power Electronics & The new energy and new power system**

Chair **Prof. Min LU**

671 18:15-18:30
Simulation on Microstructural Evolution under Electromigration in Backside Power Delivery Network
Xin Zeng
Sun Yat-sen University

694 18:30-18:45
Synergistic Effect of Current Stressing and Temperature Cycling on Reliability of Low Melting Point SnBi Solder
Zesheng Shen
City University of HongKong, China

701 18:45-19:00
Electromigration behavior study of fine pitch Cu-Sn micro-bump structure by finite element simulation
Zheqi Xu
School of Integrated Circuits, Tsinghua University

709 19:00-19:15
Application of ANSYS Sherlock in the fatigue lifetime evaluation of board level solder joint
Mengke Yang
Ericsson BNEW, Ericsson AB, Beijing, China

724 19:15-19:30
Case analysis on the fracture of deformed leads of the ceramic flat package
Zhibin Wang
China Aerospace Components Engineering Center

731 19:30-19:45
The crack propagation analysis in an IGBT package under in-service conditions by VCCT
Zhao Fu
Department of Materials Science, Fudan University

736 19:45-20:00
A New Failure Mode Induced by Coupling Effect of Electromigration and Joule Heating in Advanced Packaging
Yifan Yao
City University of Hong Kong, China

443 20:00-20:15
Computational and experimental study of a novel L-cysteine hydrochloride leveler for copper electroplated via fill in redistribution layers
Yu Jiao
Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS

452 20:15-20:30
Ad/desorption mechanism of amine-terminated polyoxypropylene suppressor in advanced acid copper electroplating
Ning Zhang
Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS

ORAL SESSION 27

Friday, August 11th, 2023 18:15 ~ 20:30

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 27

Venue **Room 6**

Session **Emerging Technologies & Applications of Electronic Technology for Artificial Intelligence**

Chair **Prof. Yanhong TIAN**

Keynote 18:15-18:45

Low-temperature solid-state bonding for chip interconnection

Prof. Hongjun JI

Harbin Institute of Technology, Shenzhen

618 18:45-19:00

A low power consumption fractal microchannel heat sink based on hierarchical ribs

Yongjin Wu

Shanghai Jiao Tong University

662 19:00-19:15

Transparent Metal Grid Electrodes Prepared by Electrohydrodynamic Printing Technology

Jingxuan Ma

Harbin Institute of Technology

677 19:15-19:30

Stealth dicing of SiC using femtosecond laser Bessel beam

Shaowei Li

Faculty of Materials and Manufacturing, Beijing University of Technology

737 19:30-19:45

Research on Heat Dissipation Technology of GaN Power Amplifier Based on Diamond Carrier

Lixiang Zhang

The 13th Research Institute of CETC

ORAL SESSION 28

Friday, August 11th, 2023 18:15 ~ 20:30

Note: Only the affiliation information of the first author is provided due to the space constraints.

Oral Session 28

Venue **Room 7**

Session **Packaging Materials & Processes & Packaging Design & Modeling**

Chair **Prof. Caifu LI**

629 18:15-18:30

Glycine-Modified Boron Nitride/Epoxy Composites with High Thermal Conductivity and Low Coefficient of Thermal Expansion

Zhen'An Dou

Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences

646 18:30-18:45

Additive fabrication of 3D surface conformal circuits using a modified screen printing technology

Wenbo Li

State Key Laboratory of Advanced Welding and Joining, Harbin Institute of Technology (Weihai)

722 18:45-19:00

Preparation of Nano-foam sheet and Its Application in High Temperature Resistance Packaging of Power Chips

Hongqiang Zhang

Beihang University

440 19:00-19:15

Effects of additive interactions on electroplating profile of IC substrate copper pillars

Xiao Li

Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS

442 19:15-19:30

Prospective application of nanotwinned copper for Damascene via filling and hybrid bonding

Li-Yin Gao

Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences

717 19:30-19:45

Low-noise Design for Power Delivery Network in 2.5D Integrated Microsystem

Yanling Wang

Northwestern Polytechnical University / Xi'an Microelectronics Technology Institute

726 19:45-20:00

Comparative analysis of different microfluidic cooling technologies for high performance chips

Jianyu Feng

Institute of Microelectronics of the Chinese Academy of Sciences

730 20:00-20:15

The prediction of orthotropic material properties for RDL based on effective modeling and CNN

Haozhou Wang

Department of Materials Science, Fudan University

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

Note: Only the affiliation information of the first author is provided due to the space constraints.

Area 1 (Sessions 1&2)

255 Using Stacked Inverse-Reflective Cup Structure to Improve Vertical Light Output and Ambient Contrast Ratio of Light Emitting Diode Display Device *Chonghui He* National and local joint engineering research center for semiconductor display and optical communication devices, South China University of Technology	4 Effect of Er and Ni-CNTs on the interfacial reaction and growth behavior of Sn58Bi/Cu intermetallic compound layers *Li Qi* Guangdong Welding Institute (China-Ukraine E.O.Paton Institute of Welding)
303 Optimizing surge current capability of small-signal SBD device based on Fan-out Panel Level Packaging *Xudong Luo* Shenzhen Siptory Technology Co., Ltd.	44 Enabling Zero Delamination between Lead Frame Surface and Epoxy Molding Compound at Zero Hour and MSL1 in Leaded Package *Wenhao Lan* Package R&D, Nexperia China Ltd, Dongguan City, Guangdong Province, China
322 Laser Etching Process of TSV and Reliability Analysis of TSV-based IC structure by Finite Element Simulation *Liyuan Zhang* School of Microelectronics Dalian University of Technology	67 In situ nondestructive study interface aging mechanism of polymeric materials/nanocomposites based on dual-beam Raman spectroscopy *Yuan Liu* Shenzhen Institute of Advanced Electronic Materials
361 Design and Integration Approach of Low-Inductance Vertical Interconnection Structure for Gallium-Nitride High Electron Mobility Transistors *Yinxiang Fan* School of Mechanical and Electrical Engineering, Guilin University of Electronic Technology	88 Development of Thermal Resistant Temporary Bonding Material for Fan-out Wafer Level Packaging: Dual-curing and Dual-debonding Strategies are Available *Kang Li* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS
449 Thermal analysis of TSV with design factors *Seong-Won Seo* Electronic Packaging Research Center, Kangnam University, Yongin-si, Korea	92 Improving Moldability by Regulating Thixotropy of Epoxy Molding Compounds *Xiang Liu* Shanghai DOiTECH Semiconductor Materials Co., LTD.
454 3D FO package technology using bridge die for high number of chiplets integration *Jiaming Zhuang* Tongfu Microelectronics Co., ltd.	129 Effect of Filler Particle Size and Surface Functionalization on the Properties of Thermal Grease *Xiangliang Zeng* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology
492 Demonstration of a wafer-level integration for System-on-Wafer Architecture *Weihao Wang* Intelligent Network Research Institute, Zhejiang Lab	163 Sidewall Chipping Investigation & Challenges on 100um Thin Low-K Wafer with DAF *Hongbin Xia* Nexperia
515 Panel level multi chip embedded high-density packaging integration technology *Xianming Chen* Zhuhai ACCESS Semiconductor Co., Ltd.	227 Study on high power DUV LED hermetic packaging utilizing Al Thin Film interconnecting Technology *Shuaiyi Pan* School of Microelectronics, Dalian University of Technology

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

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Area 2 (Sessions 3&4)

10 A junction temperature prediction model for 3D stacked packaging chip based on thermal resistance matrix *Jiahao Liu* China Electronic Product Reliability and Environmental Testing Research Insititute	33 Improvement of the solderability of aluminum alloy, nickel, stainless steel and copper by metallization of silver and nickel for power semiconductors *Jincheng Li* University of Chongqing University
56 A fast and simple method to place sub-die under Chip-let architecture based on thermal simulation *Jiangcheng Cao* Inspur Electronic Information Industry Co., Ltd.	90 Effect of pre-welding pulse on microstructure and mechanical properties for parallel gap resistance welding joint of GaAs solar cell and Ag foil *Yuhan Ding* School of Materials Science and Engineering, Shanghai Jiao Tong University
135 Experimental validation of a simple fractional model for dynamic viscoelastic behavior of polymer-based composites *Jianfeng Fan* Shenzhen Institute of Advanced Electronic Materials	401 Accurate Assessment of Young's Modulus of Sintered Ag joints by Nanoindentation *Yuning Zhang* Shenzhen Institute of Advanced Electronic Materials
140 Simulation Application of Interconnected Structure of Microsystems Based on Artificial Neural Network Technology *Yunong Ye* Information Science Academy, China Electronics Technology Group Corporation	462 Design and Manufacture of Space Transformer for Vertical Probe Card *Fei Pan* SKY CHIP INTERCONNECTION TECHNOLOGY CO
142 Influence of Cu heat sink on heat dissipation of QFN package *Haoqin Ma* Shanghai Jiao Tong University	551 Effects of Ge addition on the growth of interficial intermetallic compounds in the Sn58Bi/Ni solder joint *Shasha Zhang* Beijing Institute of Technology
150 Design Optimization for Dual Clip Flat Lead Package Assembly by Simulation *Hing Suan Cheam* Nexperia	659 Die Attach for Microelectronic Packaging: Copper Paste Comparison Between Pressure and Pressureless Techniques *Ran Liu* The Institute of Scientific and Industrial Research (ISIR), Osaka University
222 Optimizing heat source arrangement for 3D ICs with irregular structures using machine learning methods *Xixin Rao* Nanchang University	704 Preparation of full Ni3Sn4 IMC interconnects using current driven bonding method *Zhikai Chen* Dalian University of Technology
224 An isogeometric boundary element scheme for transient heat transfer problems in electronic packaging *Yanpeng Gong* Faculty of Materials and Manufacturing, Beijing University of Technology	706 A comparative finite element analysis of board-level drop reliability of Eutectic Sn-Bi, Hybrid Sn-Bi/SAC and SAC WLCSP solder joints *Zhiyi Wang* Dalian University of Technology

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

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Area 3 (Sessions 5&6)

195 A Subpixel Edge detection algorithm to test the accuracy of Semiconductor Packaging Equipment *Shikang Jin* Guangdong University of Technology	6 Theoretical Studies and Root Cause Identification of the Pinhole Defects on Al Bondpads in Wafer Fabrication and Packaging Processes *Younan Hua* Wintech Nano-Technology Services Pte Ltd
209 Research on Genetic Algorithm for Feedforward Parameter Tuning in XY motion platform *Wei Zhou* Guangdong University of Technology	12 Copper Raw Material with Elongation Factor to Improve Delam Performance *Linda Li* Nexperia
219 Research on Sliding Mode Control Algorithm of PMSLM Based on Fuzzy Switching Gain Adjustment *Huan Liu* Guangdong University of Technology	32 Studies of Atomic Force Microscopy and Application in Advanced Packaging, Materials Characterization and Failure Analysis *Hua Younan* Wintech-nano
237 Study on the Control Method of Moisture Content in Microwave Modules *Chuanwei Wang* The 38th Research Institute of CETC	37 The effect mechanism of electron irradiation on MEMS comb-type capacitive accelerometer *Xuewei Zhao* Beijing Institute of Aerospace Control Devices
262 Research on PID parameter self-tuning and feedforward control of precision X-Y motion platform for wire bonding machine. *Wen Liang* Guangdong University of Technology	48 Effect of X-rays Irradiation on the Reliability of 850nm High-speed VCSEL *Jide Zhang* Changchun University of Science and Technology
280 Surface Plasmon-polaritons Enhanced Anisotropic Etching Enabling Efficient Processing of Gallium Nitride Nanowires Arrays *Pengfei Yu* Guangdong University of Technology	63 Electromigration life model of copper pillar bump under Bidirectional Current Stressing *Zhiwei Fu* School of Energy and Power Engineering, Shandong University
287 UV light enhanced metal-assisted chemical etching of SiC triangular nanostructure arrays *Yiming Zhong* Guangdong University of Technology	72 Study on mechanical properties and microstructure reliability of composite solder under multiple reflow and high-temperature storage *Jiaxing Wang* Beijing Microelectronics Technology Institute
296 Laser-induced processing of thermal cloaks enabling heat shielding *Guanhai Wen* State Key Laboratory of Precision Electronic Manufacturing Technology and Equipment, Guangdong University of Technology	73 Study on Failure Modes of High Speed Optical Communication PCB *Bo Zhou* China Electronic Product Reliability and Environmental Testing Research Institute (CEPREI)

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

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Area 4 (Sessions 7&8)

11 Design and optimization of cell and multiple-zone gradient modulation field limiting ring (MGM-FLR) termination for 1700V/10A 4H-SiC merged PiN/Schottky (MPS) Diodes *Bofeng Zheng* Chongqing University	20 Characterization tests of Electrodeless Discharge Lamps for hyperspectral Spaceborne Calibration *Ziliang Pang* Xi'an institute of optics and precision mechanics Chinese academy of sciences
76 Ripple-control Multiple-port Step-down Power Converter Design in Outdoor Power Supply Application *Yuheng Gao* Chongqing University	89 Performance enhancement of GaN/AlGaN quantum well ultraviolet light-emitting diodes by a novel electron-blocking layer with graded inverted V structure *Taiping Han* School of Materials Science and Engineering, Xiamen University of Technology
80 Design and H3TRB Test on 650V SiC-JBS Diodes *Lei Lang* Chongqing University	131 Research on Modeling and IP Technology for High-Speed Optical Interconnection Interfaces in Optoelectronic Microsystems *Haoyan Wang* Information Science Academy of CETC
121 Power Supply Design and Application Based on Piezoelectric Effect *Xinxin Ma* School of Mechanical and Electrical Engineering	249 Strain Engineering for Modulating Electronic and Optoelectronic Properties of Monolayer InSe *Siyuan Xu* Southern University of Science and Technology
235 Research on Optimal Scheduling of microgrid based on alliance trading platform *Dongmei Yan* Shihezi University	251 Improving Optical and Electronic Performance of Monolayer Silicon Carbide via Metal Doping *Junfeng Li* Southern University of Science and Technology
244 Research on heat dissipation performance of double-sided cooling IGBT module *Zuoyi Huang* Faculty of Materials and Manufacturing, Beijing University of Technology	306 FDTD Simulation of anti-reflective performance for theSiO2/PDMS transparent packaging materials *Tengda An* University of Science and Technology of China; Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences
332 Design and Implementation of FPGA-based Digitally Controlled Quadratic Buck Converter *Honglei Cen* Shihezi University	316 The preparation of high-quality W-LED package with Sr3-xAl2Si3O12:xEu2+ and YAG:Ce3+ *Junlin Xue* Xiamen University of Technology
357 Simplified Evaluation on cooling Performance of Silicon Microfluidic Interposer *Miao Yu* Nanjing University, Nanjing Electronic Devices Institute	317 Full-spectrum White Light-emitting Phosphor-in-glass for blue LED chips by adding Green-Emitting CaY2ZrScAl3O12 :Ce 3+ Phosphor *Sicheng Yi* Xiamen University of Technology

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

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Area 5 (Sessions 9&10)

384 Implantable flexible temperature sensor for in-operando sensing of Lithium-ion batteries *Dengji Guo* School of Materials and Energy, University of Electronic Science and Technology of China	191 Flexible pressure sensor based on double-sided pyramidal microstructure *Jiantao Zeng* Zhejiang University of Technology
465 Optimization of Mason Model in thin Film Bulk Acoustic Resonators with an extra Passivating Piezoelectric Structures *Bo Wen* Peking University	225 Fine Pitch Wafer-to-wafer Hybrid Bonding for Three-Dimensional Integration *Jiang Xiaofan* Xiamen University
582 Finite Element modelling of a MEMS piezoelectric pressure sensor using FreeFem++ *Xiyao Du* Harbin Institute of Technology	429 Study on the Effect of Manual Splitting on Thermal Fatigue Reliability of PBGA Solder Joints *Xiaochuan Xie* GuangZhou Risong Intelligent Technology Holding Co., LTD.
708 Optimal design of the package with stress-buffering structure for the thermal stability improvement of MEMS resonant accelerometer *Bie Xiaorui* Aerospace Information Research Institute of Chinese Academy of Sciences	487 Wafer-level controllable graphene transfer and electrical characterization *Lu Cheng* United Microelectronics Center Co., Ltd. (CUMEC)
728 A Micro-hotplate for MEMS Gas Sensor Wafer Level Packaging *Zhaohua Zhang* Beijing Institute of Aerospace Control Devices	510 A Stochastic Resonance Bistable System based Noise Filtering Method for ADC *Ying Zhang* School of Information Engineering, Guangdong University of Technology, Guangzhou
5 A Critical Assessment of Graphene Based Heat Pipes for Electronics and Power Module Cooling Applications *Zhiyang Shen* SMIT Center, School of Mechatronics Engineering and Automation, Shanghai University	511 The EBG Structure for Mutual Coupling Suppression Between Antenna Units *Dan Xie* School of Information Engineering, Guangdong University of Technology, Guangzhou
15 3D stacking technology and TSV technology analysis *Hui Xuan* Tongfu Microelectronics Co., Ltd.	587 A ReaxFF molecular dynamics study on the mechanism of material removal from 4H-SiC substrate in chemical mechanical polishing *Lianghao Xue* School of Power and Mechanical Engineering
167 Temperature prediction model of sheep barn in winter based on Neural Network *Honglei Cen* Shihezi University	592 Design of Fuzzy Decoupling Control System for Indoor Environment *Zichen Liu* Shihezi University

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

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Area 6 (Session 2)

228 Preparation and sintering performance of micro-nano hybrid copper particles for third-generation semiconductor package interconnects *Kai Yang* State Key Laboratory of Precision Electronic Manufacturing Technology and Equipment,Guangdong University of Technology	335 The Densification Behavior and Microwave Dielectric Properties of the CBS Glass-ceramics for LTCC Application *Zhaojun Li* Shenzhen Institute of Advanced Electronic Materials
229 Epoxy adhesive of high Tg for electronic packaging with stress relaxation and self-healing *Hui Xu* University of Science and Technology of China; Shenzhen Institute of Advanced Electronic Materials	353 Study on the effects of surface hydroxyl of silica fillers on the mechanical properties of underfills *Zhenguo Zhang* Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences; University of Science and Technology of China
231 Improving the interface bonding strength of epoxy adhesives for electronic packaging *Yanzhe Luo* University of Science and Technology of China; Shenzhen Institute of Advanced Electronic Materials	364 Effect of Solder Thick on the Interfacial Reaction in Cu/Sn/Ni Solder Joints *Wangrong Liang* School of Materials Science and Engineering Jiangsu University of Science and Technology
253 Key Factors for The Formation of Intermetallic Compound During TLPB Process *Yuyan Ding* Shenzhen Institute of Advanced Electronic Materials, Chinese Academy of Sciences	399 Hansen solubility parameter optimization of surface modified silica filler in electronic packaging materials *Liu Yang* Shenzhen Institute of Advanced Electronic Materials, Shenzhen
295 Electroless amorphous Ni-Cu-P deposit and the interaction between Ni-Cu-P barrier and Sn solder *Jing Xing* Dalian University of Technology	404 Effect of Different Proportions and Powder Sizes of Sn on The Performance of Cu-Sn TLPB Joints *Yuyan Ding* Shenzhen Institute of Advanced Electronic Materials
304 Newly designed colloidal silica for copper chemical mechanical polishing in electronic packaging *Jianhang Yin* Shenzhen Institute of Advanced Electronic Materials	407 Effect of Silane Coupling Agent on The Performance of Electrically Conductive Adhesives *Mengmeng Chen* Shenzhen Institute of Advanced Electronic Materials
308 The low Dk, Df surface modification of silica filler in the high speed and high frequency applications *Qianqian Qiang* Shenzhen Institute of Advanced Electronic Materials	413 A Study on Warpage Behavior of Underfill in Flip Chip *Xiaohui Peng* Shenzhen Institute of Advanced Electronic Materials Shenzhen Institute of Advanced Technology
321 Effect of Cu content in the Ni-Cu alloy on the interfacial reaction between Ni1-xCux Alloy and Sn solder *Xiaofu Li* Dalian University of Technology	439 A Single-layer Photosensitive Polymer Material for Temporary Bonding and Laser Debonding *Xuefan Wang* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

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Area 7 (Sessions 1&2)

549 A novel 3D packaging technology for high-reliability applications *Mifeng Liu* Shanghai Aerospace Electronic and Communication Equipment Research Institute	519 A Rapid and Selective Laser Sintering Method of Silver Nanoparticles for High Temperature Electronic Devices Packaging *Guandong Liu* School of Engineering & Physical Sciences Heriot-Watt University Edinburgh, UK
559 Design and Fabrication of a Wafer-level Interposer for System-on-Wafer Packaging Application *Chuanzhi Wang* Research Institute of Intelligent Network, Zhejiang Lab	529 Effect of the toughening agent and coupling agent on the Liquid Epoxy Molding Compound *Wei Chunxiang* SHENZHEN INSTITUTE OF ADVANCED ELECTRONIC MATERIALS
563 Fabrication of Full Glass Antenna-in-Package by Laser Transmission Welding *Yuhua Guo* The 38th Research Institute, China Electronics Technology Group Corporation	613 Effect of Embedded Atoms Distribution on the Surface of Silicon Carbide on the Wettability of Molten Aluminum Droplets at Different Temperatures *Yi Lv* Hubei University of Arts and Science
603 A Ka Band Tile T/R Module based on Silicon Packaging *Qiangwen Wang* The 38th Research Institute of CETC	614 Complicated-trajectory Compartment EMI Shielding in SiP Modules by Dispensing Technology *Xiaofei Zhang* Shenzhen Institute of Advanced Electronic Materials
651 Research on TSV Stress of Ultra-thin Optical Fingerprint Chip *Jinjin Hu* Sky Chip Interconnection Technology CO., LTD	687 Design strategies of nanofillers in photosensitive polyimide nanocomposites *Tao Wang* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS
698 Research of Super Fine Gold Wire Bonding *Ting Wei* Nanjing Research Institute of Electronics Technology	688 Enhancing the Thermal Stability of Ni UBM through Introducing High-Density Nano-Twins *Yang Wu* Xi'an Microelectronics Technology Institute
741 Research on Local Heating of Flat Plate Based on Electric Field Distribution Regulation *Haojie Liu* College of Electromechanical Engineering, Changsha University	689 Influence of Cu Nanoparticles on the Microstructure of IMCs between Sn/Cu solder joint during isothermal stage of soldering *Shengyan Shang* Guizhou Institute of Technology
504 The Effect of Epoxy Molding Compound Dispensing Uniformity on PoP Warpage *Tao Pan* ChangXin Memory Technologies, Inc.	690 Effect of TiO2 Nanoparticles on growth behavior of IMCs between Sn/Cu solder joint during isothermal stage of soldering *Tianyu Xiao* Guizhou Institute of Technology

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

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Area 8 (Sessions 3&4)

248 A Comprehensive Study of Interface Damage at the Cu/Polyimide Interface in Redistribution Layers of Fan Out Wafer Level Packaging *Shilu Zhou* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS	570 Prediction of Packaging Induced-Warpage for a 3D Stacked Package with a Cure-depedent Viscoelastic Model for EMC *Han Wang* Guilin University of Electronic Technology
346 A 3D Crystal plasticity finite element model for 3D package under drop impact *Shijiao Liu* Nanjing University of Posts and Telecommunications	573 Embedded wafer-level microfluidic cooling designs for the system on wafer packaging *Jie Li* Research Institute of Intelligent Network, Zhejiang Lab
398 Development and Prospect of Coaxial Through-Silicon Via in 3D Integrated Circuits *Junkai Ma* Xidian Univ, Sch Microelect	639 Study on grinding of Cu-Ta interface based on molecular dynamics *Zhiqiang Tian* Wuhan University
405 A V band ball grid array interconnection design of ceramic package with high-performance *Yangfan Zhou* The 13th Research Institute of CETC	707 Collapse behavior and interfacial reaction of Cu-cored solder balls experienced multiple reflow soldering processes *Mingqi Yuan* Dalian University of Technology
438 Thermal and Reliability Study of Self propagating Reaction Interconnects in Microsystem Integration *Tao Zhang* Beijing Microelectronics Technology Institute	711 Electromigration-induced failure behavior of Cu/Sn-57.0Bi-1.0Ag/Cu solder joints. *Li Li* Dalian University of Technology
448 Branched Al2O3 thermally conductive epoxy materials and finite element simulation *Xiong Yao* Guilin University of Electronic Technology	712 Microstructural evolution and thermal fatigue reliability of Ni/Sn-Ag-Cu/Sn-Bi/Cu hybrid BGA solder joints assemblied by low-temperature soldering *Shanhong Liu* Dalian University of Technology
481 A Novel Band-pass Filter in Ka Band with SiP Packaging *Junjie Qin* Guilin University of Electronic Technology	713 Wafer bumping of Sn-Ag micro-bumps with high coplanarity *Na Li* Dalian University of Technology
530 Simulation and Analysis of Temperature Cycle Failure at MLCC Welding End *Yaoyao Liu* The 13th Research Institute, CETC	718 Transmission Structures Using Parylene C and TSV for Silicon-based Low-loss and Low-profile Heterogeneous Integrations at Ka-band *Qi Wang* Peking University Shenzhen Graduate School

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

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Area 9 (Sessions 5&6)

325 Completely Filling of Through-Silicon-Vias with High Aspect Ratio by High Cavity Physical Vapor Deposition and Electroplating *Manyu Wang* Xiamen University	74 Optimized stencil opening to increase solder flowing distance for solder void improvement *Jingwen Gan* Nexperia
391 Design and characterization of a novel low temperature wafer level bonding technology *Chunsheng Zhu* Strategic Support Force Information Engineering University	81 Microstructural Evolution and Shear Properties Degradation of Tin-Lead/Copper Solder Joints at Cryogenic Temperatures *Hao He* Chongqing CEPREI Industrial Technology Research Institute Co., Ltd.
392 Research on NonLinear Active Disturbance Rejection Controller for Permanent Magnet Synchronous Linear Motor *Huan Rao* Guangdong University of Technology	103 Effect of Young's modulus on the reliability of sintered silver joints: simulation and experiment *Kuifu Cheng* Shenzhen Institute of Advanced Electronic Materials
561 Enhanced energy storage performance of Na0.94Sm0.02NbO3 ferroelectric ceramics by Bi0.5La0.5Ba2/3Ta1/3O3 doping *Yaoyao Yun* Shihezi University	124 Strain Threshold Test and Case Analysis of THT Component *Wanchun Tian* China Electronic Product Reliability and Environmental Testing Research Institute
627 A novel lead-free NaNbO3-based relaxation ferroelectric ceramics for energy storage application *Jiaming Xiao* School of Mechanical and Electrical Engineering Shihezi University	145 Case Analysis and Improvement of Silver Migration in Resistors *Chaohui Hu* China Electronic Product Reliability and Environmental Testing Research Institute
665 Manual bidirectional dislocation flip chip alignment technology based on image preprocessing *Ye Lezhi* Beijing University of Technology	152 Chlorine and sulfur effects on silver bonding wire reliability *Lois Liao* Wintech-nano
679 Research on p-GaN/AlGaN high sidewall verticality and low damage etching applied to enhanced GaN HEMTs devices *Gao Xiaoxiao* College of Optoelectronic Engineering, Chongqing University of Posts and Telecommunications	173 Application research of PFMEA technology in the thermosonic gold wire bonding process *Xiaoran Cheng* China Academy of Space Technology, China Aerospace Components Engineering Center
681 Simulation study of silicon carbide scratching process with double diamond abrasive *Kunzhou Wu* Faculty of Materials and Manufacturing, Beijing University of Technology	194 Time-of-Flight Mass Spectroscopic Studies of Non-Stick on Pad Issues in Wire Bonding *Lei Zhu* Wintech Nano-Technology Services Pte. Ltd., 10 Science Park Road, #03-26, Singapore 117684, Singapore

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

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Area 10 (Sessions 7&8)

446
Research on the improved FCS-MPC strategy for Photovoltaic grid connection Based on the O-Z source inverter
Xu Weiqi
Shihezi University

746
Study on surge current characteristic of SiC SBD with different solder layer structure
Zheng Hu
Beijing Institute of Technology; Institute of Microelectronics of Chinese Academy of Sciences

566
Optimizing Temperature and Flow Fields of 4H-SiC Epitaxial Growth by Integrating CFD Simulation with Multi-objective Particle Swarm Optimization
Jing Tian
Fudan University

380
A Novel IGZO-TFT Device With High Dielectric Constant Sandwich Structure Gate Dielectric Layer
Yan Wang
School of Materials Science and Engineering, Xiamen University of Technology

628
Thermal Reliability Analysis of High-Power Terahertz Traveling Wave Tube
Shuanzhu Fang
China Electronic Product Reliability and Environmental Testing Research Institute

602
Investigation and optimization of an integrated electro-optic modulator driver with a high bandwidth package for high speed optoelectronic interconnection
Yu Ban
Information Science Academy of CETC

680
Research on Energy Shifting Benefits of Hybrid Wind Power and Concentrating Solar Power System Based on Time-of-use Electricity Price
Hong Zhang
Shihezi University

620
Hybrid integrated packaging of an optical-to-microwave converter
Yilong Wu
The 29th Research Institute of China Electronics Technology Group Corporation

693
Research on electric vehicle charging load management strategy based on Elman neural network for short-term wind and solar power prediction
Rongrong Li
School of Mechanical and Electrical Engineering, Shihezi University

729
Integrated Data Acquisition Module based on CPO packaging
Xiaomeng Lyu
The 29th Research Institute of China Electronics Technology Group Corporation

700
Design of Spacer in SiC Double-Sided Cooling Packaging Based on Multiphysics Finite Element Topology Optimization
Zizhen Cheng
Xi'an Jiaotong University

715
Simulation of Crack Initiation and Propagation in Solder Layer of IGBT Module under Temperature Shock in 3D Model Based on Phase Field Method
Qin Jiaolong
Huazhong University of Science and Technology

723
Study on Energy Management Strategy for Optical Storage Microgrid Considering Dynamic Load Fluctuation
Fuyuan Yao
School of Mechanical and Electrical Engineering, Shihezi University

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

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Area 11 (Session 6)

196 Thermo-Mechanical Fatigue Failure Simulation and Life Prediction of Solder Joints Using the Maximum Entropy Fracture Model *Xing Chen* School of Mechanical Engineering, Zhejiang University of Technology, Hangzhou	362 A Thermo-mechanical Coupled 3D Crystal Plasticity Finite Element Model for CASTIN Solder Alloy *Yang Li* Nanjing University of Posts and Telecommunications
217 The Thermal Transient Measurement for the Carbon Fiber-based Thermal Interface Materials in Electronic Packaging Structures *Yunsong Pang* Shenzhen Institute of Advanced Electronic Materials, Chinese Academy of Sciences	365 Study on Failure Mode of Asymmetric Trench SiC MOSFETs under Avalanche Stress *Shaogang Wang* Department of Electromechanical Engineering, Guilin University of Electronic Technology, Guilin, 541004, China
250 Study on the Correlation between the Ball Collapse Height and the Coplanarity Control Requirements for PBGA Reflow Soldering *Guanghui He* The Fifth Electronics Research Institute of Ministry of Industry and Information Technology	369 Common Failure Phenomenon of Microwave Components/Modules in Quality Inspection and Measures of Process Improvement *Sha Tang* China electronic product reliability and environmental testing research institute
252 Study on Electromigration Lifetime of Ni/solder/Cu Sandwich Structure with Different Pb Content *Jiang Xie* The Fifth Electronics Research Institute of Ministry of Industry and Information Technology	394 In-situ observation of microscale crack-tip strain field evolution in underfill with different toughening agents via SEM-DIC coupled method *Xuecheng Yu* Shenzhen Institute of Advanced Electronic Materials, Chinese Academy of Sciences
267 Improve the high-temperature reliability of epoxy encapsulation with copper substrates through a copper thiolate complex layer *Shuaijie Zhao* Osaka University	395 The investigation of threshold voltage instability of p-GaN AlGaN/GaN HEMT caused by the measurement *Zongqi Cai* National Key Laboratory of Science and Technology on Reliability Physics and Application of Electronic Component
269 Simulation of morphology evolution and pore segregation of Ag sinter joint at high temperature *Ye Wang* The School of Reliability and Systems Engineering, Beihang University	396 The Study on Bulging Mechanism of Plastic Packaging Materials for Electronics *Jiabao Gu* The Fifth Electronics Research Institute of Ministry of Industry and Information Technology
352 Warpage behavior of the flip chip package in underfill curing process: in situ characterization and numerical simulation *Yixuan Fan* USTC,Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences	412 Optimization and Analysis of Constant Acceleration Test Fixture for Large Size Ceramic Shell *Huixin Zhang* The 13th Research Institute of China Electronics Technology Group Corporation

355 A Comprehensive Study on signal integrity of build-up film applied to IC substrate *Cheng Zhong* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology	415 Chlorine and sulfur effects on PdCu bonding wire bHAST reliability *Lois Liao* Wintech-nano

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

Note: Only the affiliation information of the first author is provided due to the space constraints.

Area 12 (Sessions 2&3&6)

703 The Effect of Etching Lead frame on QFN Package Delamination *Yun Li* Nexperia	714 Investigation on the Influence of Frame Structure on Substrate Stress in IGBT Modules *Xiaodong Li* Hefei University of Technology
721 Study on Effect of Sintering Temperature on Decomposition Process of Organic System and Evolution of Sintered Tissues *Liang Wang* Beijing Institute of Smart Energy	645 Reliability Prediction of PBGA Solder Joint under High Temperature Torsional Composite Loading Based on BP Neural Network *Shoufu Liu* China Electronic Product Reliability and Environmental Testing Research Institute
742 Double-decker silsesquioxane-doped benzocyclobutene functionalized siloxane polymer for low k materials *Jianhao He* Fudan university	653 The reliability study on electrochemical migration evaluations for common substrates in power electronics *Mingkun Yang* Beijing Institute of Technology
744 Board Level Underfill Solution for Chiplet Design and Heterogeneous Integration package *Qingxu Yang* Henkel	657 Study on the effect of solder flux on the reliability of ceramic Package Joints *Zhen-Tao Yang* The 13th research institute of CETC
747 A case study of intermetallic evolutions in a solder joint under electromigration using a novel experiment-simulation combined approach *Haiyang Yuan* Beijing Institute of Technology	696 Study on reflow warpage deformation of high pin density BGA devices affected by moisture *Haoyang Xu* Huazhong University of Science and Technology
655 Research on Structure Reliability Design Technology of High Power Ceramic Based Microsystem package *Zhen-Tao Yang* The 13th research institute of CETC	702 Research on Acceleration Test Model and Parameter Determination Method of Integrated Circuit *Chuanjin Deng* China electronic product reliability and environmental testing research institude
656 Research on Thermal Resistance Simulation and Testing Technology of Ceramic Packaging Package *Zhen-Tao Yang* The 13th research institute of CETC	27 Board Level Solder Joint Thermal Fatigue Reliability Improvement by Optimizing PCB Pad Size and Solder Paste Stencil Mask Designs *Hongbin Shi* Huawei Technologies Co., Ltd
685 Effect of current on the growth of intermetallic compounds in Sn-3.0Ag-0.5Cu solder joints *Li Bofeng* Northwestern Polytechnical University	

POSTER SESSION

Friday, August 11th, 2023 11:45~12:15 / 17:45~18:15

Note: Only the affiliation information of the first author is provided due to the space constraints.

Area 13 (Session 6)

418 Effect of Chip Size and Shape on The Thermal Stress and Strain of Sintered Ag Joints During Thermal Cycling *Yuning Zhang* Shenzhen Institute of Advanced Electronic Materials	548 Research on the Application of Microscopic Analysis Technology in PCB Inspection and Failure Analysis *Zhenhai Chen* China Electronic Product Reliability and Environmental Testing Research Institute
436 Failure analysis and modeling of blind vias crack in BGA-PCB assemblies *Shi Ying* Guangdong University of Technology	550 Investigation on the effect of the packaging-induced stress on the reliability of a MEMS sensor package *Danyang Chen* Guilin University of Electronic Technology
447 Simulation of performance and reliability of nano-copper paste in power device packaging *Tongtong Wang* Shenzhen Institute of Advanced Electronic Materials	555 Characterization and modeling of interface delamination in 3D stacked package with combination of experimental and CZM analysis *Cheng Zhu* Guilin University of Electronic Technology
455 The Influence of Heterogeneous RDL on the RF characteristic of Millimeter wave Phased Array Microsystem *Lichang Huang* School of Electronics and Information, South China University of Technology	558 Warpage Analysis and Optimization of Fan-Out Panel-Level Packaging in Hygrothermal Environment *Zijian Wang* Guilin University of Electronic Technology
456 Reliability Analysis and Evaluation of Epoxy Resin Adhesive for LED Encapsulation *Huanxiang Xu* The Fifth Electronics Research Institute of Ministry of Industry and Information Technology	581 Research on Board Level Reliability of Mounted Ceramic Package *Zhang Qian* The 13th Research Institute of China Electronics Technology Group Corporation
475 Analysis of the influence of dispensing on the reliability of CCGA solder joints *Xiaodong Chen* China Electronic Product Reliability and Environmental Testing Research Institute (CEPREI)	595 Reliability influence of solder joints on gold plated carriers *Linjiang Tang* Beijing Spacecrafts，China Academy of Space Technology
503 Research on Packaging Reliability of LTCC High Density Packaging Substrate with High-CTE *Han Li* The 13th Research Institute, CETC	607 Influence of voids in solder layer on the interconnection reliability of IGBT chip and substrate under temperature shock *Danlei Jiang* Huazhong University of Science and Technology
527 Effect of metal ions on corrosion behavior of component coating in high temperature and humidity environment *Haoxi Fu* China electronic product reliability and environmental testing research institute	632 Study of Residual Stress in Packaging Process on Solder Joint Life under Thermal Shock *Chang Yu* Faculty of Materials and Manufacturing, Beijing University of Technology

CONFERENCE GUIDELINE

Welcome to ICEPT 2023. Please read this guideline carefully, we will be more than happy to serve you.

1 Please always wear your conference pass during the conference period.

2 Meal time and location during the conference (Coupon needed).

Date	Time	Location	
Thursday, August 10th	12:20--12:50	Tea Break	North District Hall
	14:10--15:40	Lunch	Fangyuan Cafeteria
	17:25--17:55	Tea Break	North District Hall
	20:00--22:00	Welcome Dinner	Grand Link Hotel
Friday, August 11th	11:45--12:15	Tea Break	Boxue Building
	14:00--15:30	Lunch	Fangyuan Cafeteria
	17:45--18:15	Tea Break	Boxue Building

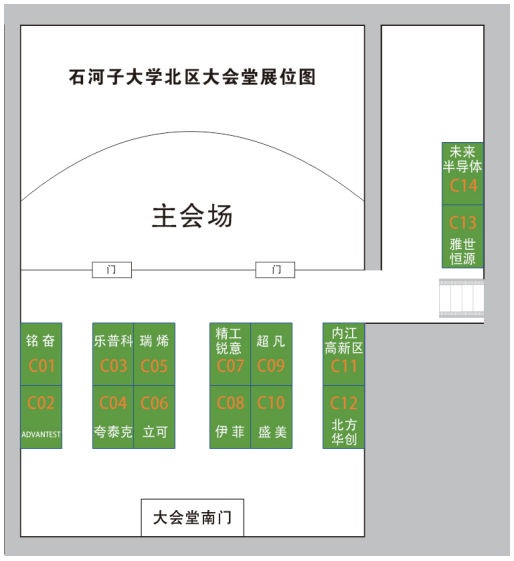
3 Please take care of your valuables including cell phones, laptops and wallets.

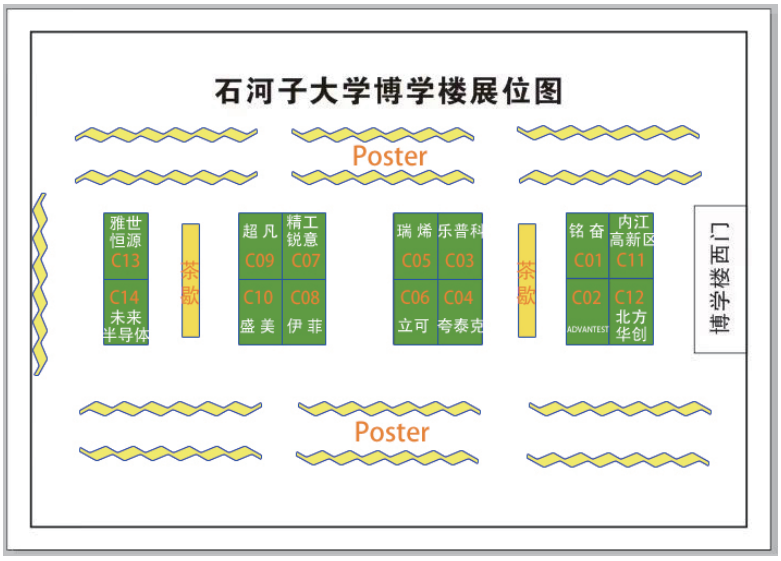
4 Delegates staying at the Grand Link Hotel please meet in the hotel lobby at 9:30 am on 10/11 August, and you can arrive at the conference venue by chartered bus.

5 During the conference, please switch your mobile phones to silent mode and help to maintain good order in the auditorium.

6 Location of Exhibition: August 10th : South lounge of North District Hall, August 11th : 1F Boxue Building.

7 Paper posting time: August 9-10th , 10:00--20:00, Location: 1F Boxue Building.





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·ON-SITE REGISTRATION

Venue1: Academic Exchange Center, Shihezi University (Only for August 8th)

Venue 2: Grand Link Hotel (August 8-10th)

Venue 3: Boxue Building, Shihezi University (Only for August 9th)

Note:

1 The Grand Link Hotel is about 5 minutes' drive from the South Gate of the northern part of Shihezi University.

2 Aipai International Hotel is about 10 minutes' drive from the South Gate of the northern part of Shihezi University.

·LAYOUT OF CONFERENCE VENUE

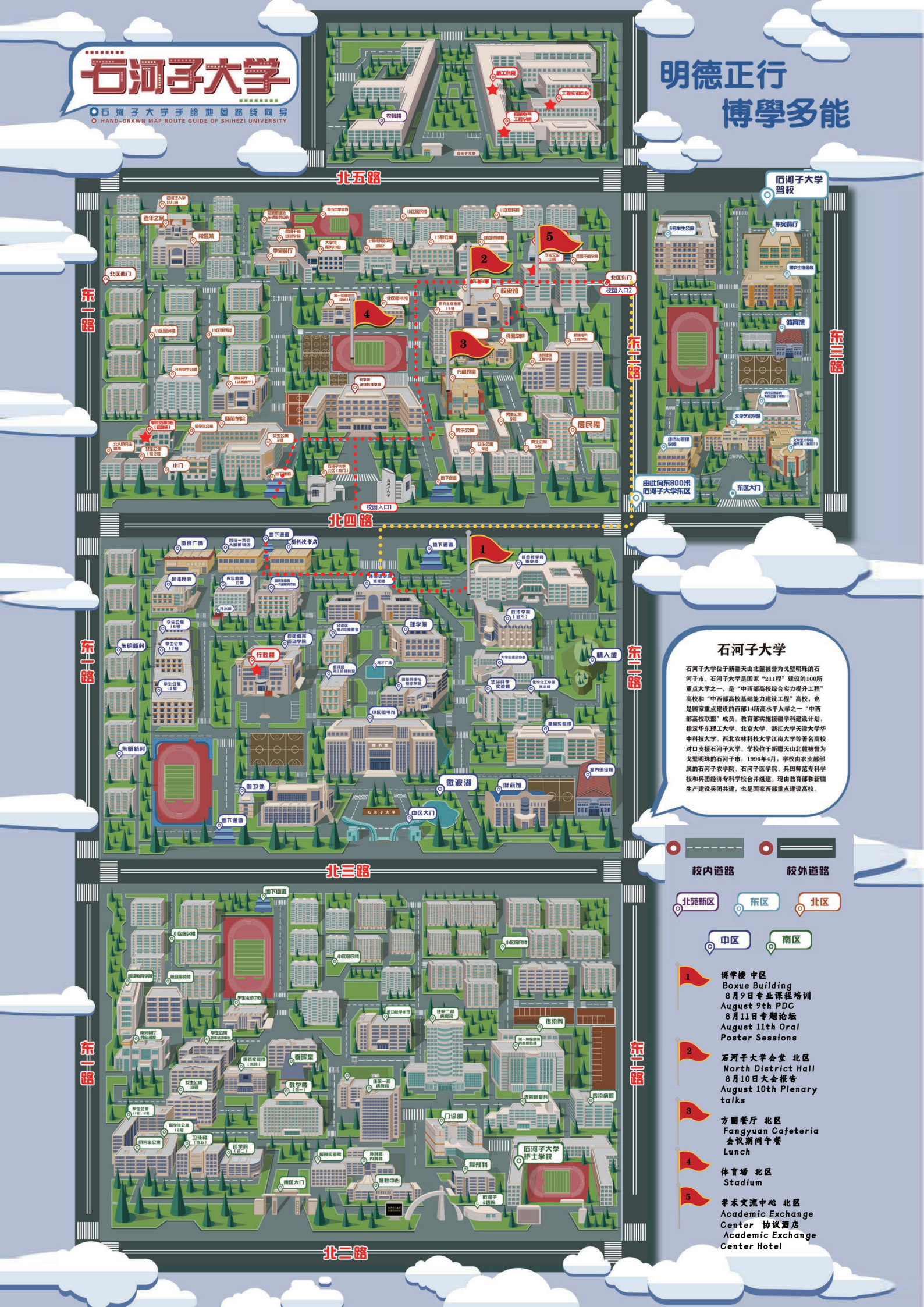
Date	Venue	
Wednesday, August 9th	PDC	Boxue Building
Friday, August 11th	Oral & Poster Sessions	
Wednesday, August 9th	Football Game	Stadium
Thursday, August 10th	Opening Ceremony Plenary Talks	North District Hall
Thursday, August 10th	Welcome Dinner	Grand link hotel, Shihezi

石河子大学

石河子大学手绘地图路线图导

HAND-DRAWN MAP ROUTE GUIDE OF SHIHEZI UNIVERSITY

明德正行
博學多能



石河子大学

石河子大学位于新疆天山北麓被誉为戈壁明珠的石河子市。石河子大学是国家“211程”建设的100所重点大学之一，是“中西部高校综合实力提升工程”高校和“中西部高校基础能力建设工程”高校，也是国家重点建设的西部14所高水平大学之一“中西部高校联盟”成员。教育部实施援疆学科建设计划，指定华东理工大学、北京大学、浙江大学天津大学华中科技大学、西北农林科技大学江南大学等著名高校对口支援石河子大学。学校位于新疆天山北麓被誉为戈壁明珠的石河子市，1996年4月，学校由农业部部属的石河子农学院、石河子医学院、兵团师范专科学校和兵团经济专科学校合并组建。现由教育部和新疆生产建设兵团共建，也是国家西部重点建设高校。

1 博学楼 中区
Boxue Building
8月9日专业课程培训
August 9th PDC
8月11日专题论坛
August 11th Oral Poster Sessions

2 石河子大学会堂 北区
North District Hall
8月10日大会报告
August 10th Plenary talks

3 方圆餐厅 北区
Fangyuan Cafeteria
会议期间午餐
Lunch

4 体育场 北区
Stadium

5 学术交流中心 北区
Academic Exchange Center 协议酒店
Academic Exchange Center Hotel

欢迎辞

电子封装技术国际会议（ICEPT）是国际电气电子工程师协会电子封装学会（IEEE EPS）在中国的旗舰会议之一。自 1994 年创办以来，ICEPT 已在北京、上海、深圳、西安、桂林、大连、成都、长沙、武汉、哈尔滨、中国香港、广州和厦门等地成功举办 23 届。经过 29 年的努力，ICEPT 现已成为国际电子封装领域四大学术会议（ECTC、ESTC、EPTC、ICEPT）之一。

今年，电子封装技术国际会议（ICEPT）迎来了第 24 个年头。ICEPT 2023 由石河子大学承办，由 IEEE 电子封装学会（EPS）提供技术支持。共有来自 14 个国家和地区的 700 多名代表出席本次会议，录取论文 500 余篇，涵盖 10 个专题。

本次会议的承办方石河子大学是一所高水平的综合性大学，自建校以来，为我国边疆地区的发展和人才培养做出了突出贡献。在会议筹备过程中，石河子大学为会议的成功举办付出了大量心血，在此，我向他们表示感谢。

除了课程培训、主旨报告、特邀报告、口头报告、海报和展览等常规环节外，我们将根据往届会议的经验，继续将线下和线上平台相结合，最大限度地提高本次会议的影响力，为国内外专业人士和研究人员提供一个交流平台。在此，我还要向在会议宣传、稿件审核和筹备过程中辛勤付出的学术委员会、组委会和十个会场的专家们表示最衷心的感谢。

在全球集成电路和封装行业稳步发展的阶段，先进封装已成为行业增长的动力。具有国际视野的研究机构和企业应尽快驶入先进封装发展的快车道。在这一背景下，ICEPT 将共同面对机遇和挑战，继续促进研究人员和工程师之间的思想交流与合作，这不仅有助于国内高端人才的培养，也为全球电子封装技术交流做出贡献。

今年，电子封装技术国际会议将首次在我们壮美的新疆举办，我们期待着新老朋友相聚在这个美丽的边疆地区。我希望此次顶级的国际会议能够加强 IEEE EPS、IMAPS、ECTC、ESTC 和 EPTC 等国内外组织和会议之间的长期合作。欢迎您参加 ICEPT 2023，期待您的参与。

叶甜春
ICEPT 2023 大会主席

目 录

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中国科学院微电子研究所
石河子大学
国际电气和电子工程师协会电子封装学会
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专题 2 – 封装材料与工艺

主席

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专题 3 – 封装设计、建模与仿真

主席

杨道国	中国桂林电子科技大学 教授
刘丰满	中国科学院微电子研究所 教授

成员

陈 沛	北京工业大学
樊海波	安世半导体
何 虎	中南大学
卢 华	英国格林威治大学
李 君	中国科学院微电子研究所
龙 旭	西北工业大学
缪 旻	北京信息科技大学
秦红波	桂林电子科技大学
史洪宾	华为技术有限公司
单 雷	IBM
魏兴昌	浙江大学
王 珺	上海复旦大学
张童龙	华为技术有限公司
张新平	华南理工大学
Xiaowu ZHANG	新加坡微电子研究院

专题 4 – 互连技术

主席

蔡 坚	中国清华大学 教授
黄明亮	大连理工大学 材料科学与工程学院院长

成员

陈雷达	西安微电子技术研究所
陈 卓	中南大学
谷 新	中山芯承半导体
黄颖卓	北京微电子技术研究所

李望云	桂林电子科技大学
刘影夏	中国香港城市大学
刘子玉	复旦大学
马书英	华天科技（昆山）
王晨曦	哈尔滨工业大学
谢 鸿	通富微电子
Chaoqi ZHANG	美国高通
Dingyou ZHANG	美国博通
张 昱	广东工业大学

专题 5 – 先进制造技术与设备

主席

刘 胜	武汉大学动力与机械学院 院长
崔成强	广东工业大学机电工程学院 教授

成员

陈志文	武汉大学工业科学研究院
李宗怿	长电集成电路（绍兴）有限公司
陈福平	盛美半导体设备（上海）有限公司
丁培军	北京北方华创微电子装备有限公司
史海涛	长电科技
王宏杰	通富超威
朱福龙	华中科技大学
周新军	苏州旭创科技
唐 亮	唐人制造（宁波）有限公司
王云峰	大连佳峰自动化股份有限公司
叶五毛	拓荆科技股份有限公司
刘 俐	武汉理工大学

专题 6 – 质量与可靠性

主席

秦 飞	北京工业大学 教授
谢 斌	深圳市大能创智半导体有限公司 副总经理
杨晓锋	工业和信息化部电子第五研究所电子元器件可靠性物理及其应用技术国家级重点实验室先进封装与微系统可靠性 技术总师

成员

陈 思	工信部电子第五研究所
戴小平	湖南国芯半导体科技有限公司

郭宇铮	武汉大学
马海涛	大连理工大学
宁圃奇	中国科学院电工研究所
刘建辉	天芯互联科技有限公司
夏明璐	中国香港应用科技研究院有限公司
贺致远	中国赛宝实验室
代岩伟	北京工业大学
徐 莎	广东工业大学
钟 毅	厦门大学

专题 7 – 功率电子与新能源及新型电力系统

主席

叶怀宇	南方科技大学 正高级研究员、副教授
梁红伟	大连理工大学微电子学院 院长
鲁 敏	石河子大学机械气工程学院电气工程系 主任

成员

高子阳	中国香港应用科技研究院
侯召政	华为技术有限公司
李道会	上海蔚来汽车有限公司
李巍巍	南方电网科学研究院
梅云辉	天津工业大学
钱钦松	东南大学
唐新灵	国家电网智能电网研究院
于洪宇	南方科技大学
张克雄	大连理工大学
路 延	中国澳门大学
曾兆权	石河子大学
王 宾	清华大学
王海云	新疆大学
侯峰泽	中国科学院微电子研究所

专题 8 – 光电器件与封装

主席

张建华	上海大学微电子学院执行院长、教授
龙浩晖	华为 科学家
刘召军	南方科技大学 教授

成员

程宏斌	希达电子
陈 平	中国科学院半导体研究所
丁星伟	先进显示与系统应用教育部重点实验室
范亚明	中科院纳米所
Jianhui Li	华为
路秀真	上海大学
罗 一	大连理工大学
吕毅军	厦门大学
宁洪龙	华南理工大学
孙 瑜	华进半导体
陶国桥	埃赋隆半导体
陶继方	山东大学
汪炼成	中南大学
薛海韵	中国科学院微电子研究所

专题 9 – 微机电封装

主席

尚金堂	东南大学 教授
陈光雄	日月光（高级半导体工程）中央开发工程 副总裁

成员

崔 健	北京大学
蔡志匡	南京邮电大学
黄煜哲	日月光
柳辉忠	日月光
单光宝	西安电子科技大学
汤士杰	日月光
王丽熙	南京工业大学
王天驰	南京理工大学
吴宜洪	日月光
肖 克	中科院上海微系统所
赵立波	西安交通大学
孔雯雯	中国科学院新疆理化技术研究所

专题 10 – 新兴领域封装与面向人工智能的电子技术应用

主席

于大全	厦门大学 特聘教授、厦门云天半导体 创始人
田艳红	哈尔滨工业大学 材料科学与工程学院 长聘教授
高 攀	石河子大学信息科学与技术学院 副院长

成员

段国韬	华中科技大学
桂 林	中国科学院理化技术研究所
刘 磊	清华大学
林路禅	上海交通大学
马盛林	厦门大学
彭春荣	中国科学院微电子所
吴国强	武汉大学
王 尚	哈尔滨工业大学
张 敏	北京大学深圳研究生院
丁 苏	西安电子科技大学
刘长征	石河子大学

大会概览

备注：最终日程以实际为准。

日期	时间	教 室 1	教 室 2
8 月 9 日	10:00--13:30	课程-1	课程-2
	13:30--15:30	*休息*	
	15:30--19:00	课程-3	课程-4
	19:30--21:15	足球友谊赛	
日期	**时间**	**北区大会堂**	
8 月 10 日	10:00--10:30	开幕式	
	10:30--11:00	大会报告 1	
	11:00--11:35	大会报告 2	
	11:40--12:15	大会报告 3	
	12:20--12:50	*茶歇与展览交流*	
	12:50--13:25	大会报告 4	
	13:30--14:05	大会报告 5	
	14:10--15:40	午 餐	
	15:40--16:10	大会报告 6	
	16:15--16:45	大会报告 7	
	16:50--17:20	大会报告 8	
	17:25--17:55	*茶歇与展览交流*	
	17:55--18:25	大会报告 9	
	18:30--19:00	大会报告 10	
	19:00--19:35	大会报告 11	
	20:00--22:00	*欢迎晚宴*	

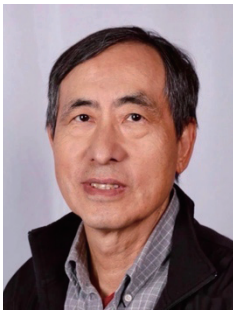
日期	时间	会场 1	会场 2	会场 3	会场 4	会场 5	会场 6	会场 7
8 月 11 日	10:00--11:45	口头报告 1	口头报告 2	口头报告 3	口头报告 4	口头报告 5	口头报告 6	口头报告 7
	11:45--12:15	*张贴报告*						
	12:15--14:00	口头报告 8	口头报告 9	口头报告 10	口头报告 11	口头报告 12	口头报告 13	口头报告 14
	14:00--15:30	*午餐*						
	15:30--17:45	口头报告 15	口头报告 16	口头报告 17	口头报告 18	口头报告 19	口头报告 20	口头报告 21
	17:45--18:15	*张贴报告*						
	18:15--20:30	口头报告 22	口头报告 23	口头报告 24	口头报告 25	口头报告 26	口头报告 27	口头报告 28
结 束								

专业发展课程

星期三 8 月 9 日，10:00-19:00 石河子大学 中区 博学楼

地 点	时 间	内 容	讲 师
教室 1	10:00-11:15 Break 11:45-13:00	***课程-1*** 先进节点芯片的先进封装解决方案	*葛维沪 博士* 美国 Pacrim 技术公司创始人兼总裁
	13:00-13:30	课程问答	
	13:30-15:30	*休 息*	
	15:30-16:45 Break 17:15-18:30	***课程-3*** 异构集成芯片封装可靠性挑战和路标	*Richard RAO 博士* 美国迈威尔科技资深首席工程师
	18:30-19:00	课程问答	
教室 2	10:00-11:15 Break 11:45-13:00	***课程-2*** 实现无铅焊点的高可靠性–从材料的角度	*李宁成 博士* 中国炫纯科技创始人
	13:00-13:30	课程问答	
	13:30-15:30	*休 息*	
	15:30-16:45 Break 17:15-18:30	***课程-4*** 微电子和封装集成的计算机辅助工艺与可靠性	*刘 胜 教授* 中国武汉大学动力与机械学院院长
	18:30-19:00	课程问答	
体育场	19:30-21:15	***足球友谊赛***	

课程讲师简介



葛维沪 博士, 美国 Pacrim 技术公司创始人兼总裁

葛维沪博士，在半导体封装和微电子组装领域拥有 40 年经验，在康奈尔大学获得硕士及博士学位，曾在汉高、摩托罗拉、金士顿技术等企业工作，葛维沪先生是 IEEE 电子封装协会 Fellow，曾任 IEEE ECTC 会议技术委员会主席，至今发表过 90 多篇技术论文，取得美国 40 多项行业技术专利。

课程方向：IC 后端封装、组装和测试（PAT）已成为延续摩尔定律以提高小节点半导体性能的实用解决方案。本课程将回顾 IC 封装技术从传统引线框/BGA 到晶圆级 3D 封装的演变，以实现异构集成和精细间距、高密度互连。使用更复杂的设计、新材料和高精度的工艺和测量技术，使得高密度先进封装技术不断发展。本课程旨在让与会者了解 IC 封装技术、应用、设计、材料和制造工艺的基本原理，这些基本原理正在高密度高级封装（HDAP）技术中取得进展，以进一步提高 10nm 以下先进节点半导体 IC 的性能。具体的主题讨论集中在晶圆级扇出的异构和 3D 集成、细间距、微凸点和混合键合、小芯片互连、新封装材料和新一代先进封装的热管理。介绍了领先的 Fab、IDM 和 OSAT 的封装案例。

李宁成 博士，中国炫纯科技创始人

李宁成博士是中国铱纯科技的创始人，在此之前，他是铟泰公司的技术副总裁。他从 1986 年到 2021 年一直在 Indium 工作。在加入 Indium 之前，他曾在 Morton Chemical 和 SCM 工作。他在 SMT 行业开发助焊剂和焊料方面拥有 30 多年的经验。他于 1981 年获得阿克伦大学高分子科学博士学位，并于 1973 年获得中国国立台湾大学化学学士学位。Ning-Cheng 是 Newnes 的“回流焊接工艺和故障排除：SMT，BGA，CSP 和倒装芯片技术”的作者，也是其他 5 本书的合著者。他获得了 SMTA 和 APEX 颁发的 5 项最佳会议论文奖。他被授予 2002 年 SMTA 杰出成员，2006 年 CPMT 杰出技术成就奖，2007 年 CPMT 杰出讲师，2009 年 SMTA 杰出作者，2010 年 CPMT 电子制造技术奖，SMTA2015 年创始人奖和 2017 年 IEEE Fellow。

课程方向：本课程涵盖了实现高可靠性无铅焊点在材料方面所需详细考虑的事项，包括焊点的机械性能、在各种材料组合和老化条件下金属互化物（IMC）的成分和程度演变，以及这些 IMC 如何影响可靠性。课程将详细讨论焊点的失效模式、热循环可靠性和在材料合成、热反应和应力反应作用下的焊点脆性；如何选择具有较低脆性的新型合金；用于汽车工业的高可靠性焊料合金的关键参数；电迁移和锡须生长也将在课程上被讨论。本课程的重点是了解各种因素如何影响失效模式，以及如何选择适当的焊料合金和表面处理以实现高可靠性的要点。

Richard RAO 博士，美国迈威尔科技资深首席工程师

Richard RAO 博士目前是 Marvell 的资深首席工程师，也是 IEEE 的高级成员。在加入 Marvell 之前，他是 Microsemi（Microchip）Corp.的研究员和 Ericsson Inc.的顾问工程师，他的职责包括开发先进电路、封装和芯片倒封装交互的可靠性流程设计。Richard RAO 博士是 IEEE-EPS（电子封装协会）可靠性技术委员会主席，并共同主持了 IEEE 异构集成路线图的可靠性路线图。同时，还是 IEEE-REPP 电子和光子学封装可靠性研讨会的总主席和技术项目主席，并担任 IEEE-IRPS（国际可靠性物理研讨会）的技术委员会主席。Richard RAO 博士，获取了中国科学技术大学固体材料力学博士学位，美国西北大学博士后研究员，研究方向为先进集成电路可靠性失效机理。在加入 Marvell 之前，曾在学术界和工业界担任可靠性物理和工程的高级技术职位。曾任中国科学技术大学副教授、新加坡国家科学技术委员会研究员。

课程方向：本教程研究了“SysMoore”的可靠性含义，即系统级异构集成（HI），它正在被开发为保持性能增长速度的一种手段，这是我们根据摩尔定律所期望的。由于 HI 的双重驱动和片上技术的进步，系统的复杂性、功能、多样性和密度不断增加，将为满足和验证客户的可靠性目标提出新的挑战。未来的多功能 HI 系统将是复杂的多尺度和多物理场系统。

刘 胜 教授，武汉大学动力与机械学院院长

1963 年 3 月出生。1992 年在美国斯坦福（Stanford）大学获得博士学位。1992 年到 1995 年在佛罗里达理工学院任教。1995 年到 2001 年任美国 Wayne 州立大学机械工程系和制造研究所终身教职，电子封装实验室主任。

2004 年 5 月到任华中科技大学特聘教授、机械科学与工程学院微系统研究中心主任。2002 年 5 月到 2006 年受聘为科技部微机电系统重大专项总体专家组成员。2006 年 11 月受聘为科技部半导体照明重大项目总体专家组成员。2009 年当选为 ASME Fellow。2013 年当选为 IEEE 会士。 2014 年 1 月受聘武汉大学动力与机械学院院长，2017 年受聘武汉大学工业科学研究院执行院长，2020 年受聘武汉大学微电子学院副院长。

大会报告议程

星期四，8 月 10 日，10:00-19:35 石河子大学 北区 大会堂

开 幕 式 **主 席：张国旗 教授 荷兰代尔夫特理工大学**	
10:00--10:30	*叶甜春* 教授 大会主席 *代 斌* 教授 石河子大学校长 *领导* 石河子市 *Kitty PEARSALL* 博士 IEEE EPS 主席
大 会 报 告 **主 席：樊学军 教授 美国拉玛尔大学**	
10:30--11:00	**半导体封装的供应链趋势、挑战和变革** *Kitty PEARSALL 博士* IEEE EPS 主席
11:00--11:35	**高性能封装创新推动微系统集成变革** *郑 力 先生* 长电科技 CEO
11:40--12:15	**适用于低温三维集成的表面活化键合** *Tadatomo SUGA 教授* 日本东京大学名誉教授，日本明星大学教授
12:20--12:50	茶歇与展览交流
12:50--13:25	**先进封装中的金属薄膜设备及工艺挑战** *耿 波 先生* 北京北方华创微电子装备有限公司 PVD 事业单元副总经理
13:30--14:05	**先进封装国产化发展趋势及产品化挑战** *李 成 先生* 中国海光信息技术股份有限公司总裁助理，主任工程师
14:10--15:40	午 餐
大 会 报 告 **主席：李世玮 教授 中国香港科技大学**	
15:40--16:10	**整体静电保护协同设计：挑战** *王自慧 教授* 美国加州大学
16:15--16:45	**面向内存计算的异构集成制造技术** *Koukou Suu 博士* 日本爱发科株式会社总裁/CEO
16:50--17:20	**用于下一代先进互连技术的混合键合** *Anton Alexeev 博士* 奥地利 EVG 公司 BD 经理
17:25--17:55	茶歇与展览交流
17:55--18:25	**CPO 的今生、前世及未来** *张 源 女士* 专家级讲师
18:30--19:00	**从电迁移到热迁移：封装设计规则的根本改变** *樊学军 博士* 美国拉玛尔大学 教授
19:05--19:35	**面向芯粒集成的先进封装技术** *王启东 博士* 中国科学院微电子研究所 封装中心主任
20:00--22:00	**欢迎晚宴 石河子恒和华星酒店**

大会特邀报告人简介

Dr. Kitty PEARSALL, IEEE EPS 主席

Kitty Pearsall 获得了德克萨斯大学冶金工程理学学士学位和机械工程与材料理学硕士和博士学位。在 IBM 41 年的职业生涯中被任命为战略制定的角色，并获得了多个奖项。2000-2013 年担任 IBM 集成供应链杰出工程师，是 IBM 技术学院荣誉退休成员，在职期间获得多项 IBM 杰出技术成就奖；12 项美国专利，还有大量 IBM 内部出版物以及 22 份外部出版物。目前，Kitty 是 Boss Precision 股份有限公司的总裁，并担任独立顾问。Kitty 是 IEEE 31 年的活跃成员，也是 EPS 28 年的成员，其角色和职责不断增加，包括 ECTC 制造技术委员会，自 2006 年起担任 ECTC PDC 主席，自 2005 年起担任 EPS/CPMT 理事会主席。

郑 力 先生，中国江苏长电科技股份有限公司 CEO

郑力，东京大学经济学硕士，天津大学工业管理工程专业工学士。郑力先生是集成电路产业领域的资深专业人士，在美国、日本、欧洲和中国的集成电路产业拥有近 30 年的工作经验。曾担任恩智浦全球高级副总裁兼大中华区总裁，瑞萨电子大中华区 CEO 等高级管理职务。目前同时担任中国半导体行业协会副理事长、中国集成电路创新联盟副理事长、中国半导体行业协会封测分会当值理事长、上海市集成电路行业协会副会长、中关村融信金融信息化产业联盟副理事长等职务。

Tadatomo SUGA 教授，日本东京大学名誉教授，日本明星大学教授

Tadatomo SUGA 教授于 1979 年加入德国马克斯-普朗克金属研究所，1983 年获得德国斯图加特大学材料科学博士学位。自 1984 年以来，他一直是东京大学的教师，且自 1993 以来一直担任工学院精密工程系的教授。他还曾担任日本国立材料研究所（NIMS）互联生态设计研究小组主任、日本科学委员会委员、IEEE CPMT 日本分会主席、日本电子封装学会（JIEP）会长。他的研究重点是微系统集和封装，以及开发互联技术，特别是用于 3D 集成的室温键合技术。他致力于在封装技术的产业界和学术界之间建立合作，指导微系统集成研究所（IMSI）的研发项目。此外，作为国际生态设计大会的主要组织者，他提倡封装技术在环境方面具有重要作用。2019 年 3 月，他从东京大学退休，加入明星大学继续从事研究工作。

耿 波 先生，北京北方华创微电子装备有限公司 PVD 事业单元副总经理

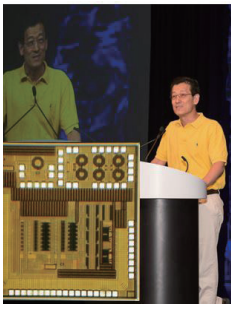
耿波，北京北方华创微电子装备有限公司 PVD 事业部副总经理，硕士毕业于河北大学等离子体物理专业。2010 年加入北方华创，主持开发了针对集成电路、先进封装、功率器件、LED 等领域的多款 PVD 设备，市场占有率在国内名列前茅。拥有授权专利 20 余篇。

李 成 先生，海光信息技术股份有限公司总裁助理，主任工程师

李成，毕业于东南大学电子工程系，历任海光产品开发运营中心副总经理及海光信息总裁助理。近 20 年半导体集成电路工作经验，具有多年在 Fairchild、AMD 等外企集成电路行业产品开发经验。2010 年即参与 2.5D Stack 工程开发，主导封测方法论及失效改善等，涵盖 CPU 及 GPU 复杂 IC 芯片硅后新产品导入及供应链管理领域。带领开发基于国产供应链的 2.5D 产品，包括传统 interposer 技术及基于 Fanout 的 RDL 技术，积极推动落实芯片设计全流程国产化。

演讲摘要：基于 2.5D 及 3D 从工程到量产的快速发展，国内相关技术迭代加快，在此过程中国内工艺厂利用后发的资金、人才优势可以加快技术发展；产品公司则从市场化角度共同推动产品化的更优技术路线，可以实现后发成本、技术优势。本文也将重点针对 2.5D 的不同技术路线的产品化验证并进行比较。同时未来在先进封装尤其是 3D 封装下，除了工艺挑战外，对产品公司也提出了更高挑战，包括产品设计、产品定义、硅后封测逻辑等，形成系统化的解决方案才能最大化利用好先进封装的优势。

演讲大纲：1.先进封装国产化发展时间线展望；2.2.5D 工艺的国产化之路的整合和选择；3.先进封装下产品设计及量产化挑战；4.国产化路线展望及总结。



王自慧 教授，美国加州大学

王自慧是美国加利福尼亚大学河滨分校电子与计算机工程系教授。研究领域包括半导体器件、模拟/混合信号和射频集成电路、集成电路可靠性设计、三维异构集成、新兴器件和电路、以及 LED 可见光通信。他出版了两本书，发表了 310 多篇同行评审论文，拥有 16 项美国专利。他担任编委的期刊包括：IEEE Transactions on Circuits and Systems I、IEEE Electron Device Letters、IEEE Transactions on Circuits and Systems II、IEEE Transactions on Electron Devices、IEEE Journal of Solid-State Circuits、IEEE Transactions on Device and Materials Reliability。他在 IEEE Electron Devices Society、IEEE Circuits and Systems Society、IEEE Solid-State Circuits Society 是 IEEE 杰出讲师。曾任 IEEE 电子器件学会主席、美国国家科学基金会项目主任、曾获得 IEEE J. J. Ebers 奖。王自慧教授是美国国家发明家科学院 Fellow 和 IEEE Fellow。

演讲摘要：静电放电（ESD）保护一直是集成电路（IC）和微电子系统（包括裸芯片和封装微芯片）中一个主要的可靠性问题。任何片上/封装内/板上的静电放电保护都不可避免地会影响系统性能。另一方面，三维异构集成（HI）技术和异构集成微系统给静电放电保护设计带来新的复杂性。因此，整体的静电放电保护协同设计对先进的微系统芯片至关重要。本文着重介绍新兴的静电放电保护设计挑战，并讨论未来芯片静电放电保护的一些展望。

Koukou Suu 博士，日本爱发科株式会社总裁/CEO

Koukou Suu 博士分别于 1988 年和 1993 年毕业于日本东北大学并获得工程学博士学位。他于 1993 年加入日本爱发科株式会社（ULVAC），此后一直致力于引领和参与众多半导体和电子技术的开发，包括新兴的非易失性存储器、高 K 电容器、LED、电源设备、薄膜锂电池以及 3D 封装制造技术。他在 2008 到 2014 年间担任公司半导体与电子技术研究所总经理。目前，他是 ULVAC 的执行官和高级研究员、ULVAC Technologies（在北美代表 ULVAC 的一家公司）的总裁兼首席执行官。他还是中国科学院上海微系统与信息技术研究所兼职教授和南澳大学的兼职工业教授。他拥有 170 多项专利（日本、欧盟、美国），发表 80 多篇行业和学术出版物。

Anton Alexeev 博士，奥地利 EVG 公司 BD 经理

他在埃因霍芬理工大学获得电气工程博士学位，并在该校获得物理学工程博士专业学位。他在半导体行业拥有多年的专业经验。他曾从事多种技术研究，曾与飞利浦照明公司合作开发 LED 可见光通信，并与 ASML 公司合作优化尖端半导体制造节点的叠层性能。

演讲摘要：晶圆对晶圆混合键合在过去十年获得极大关注，因为它在晶圆级互连制造方面具有主要优势。裸片到晶圆的工艺流程作为一种替代工艺得到开发。这种方法是建立在已知合格芯片原则基础上的：在晶圆制造之后，裸片将进行切割，通过质量标准的裸片被用于在晶圆上键合。这样，由于单个晶圆的良率损失而导致的键合良率损失将降到最低。

本文将对两种类型的混合键合进行概述，将介绍两种类型的裸片到晶圆的工艺流程，将回顾该技术的主要规格和一些主要挑战对工艺结果的影响，将强调采用新计量和调查方法的重要性。

演讲大纲:

- 混合键合简介
- 裸片到晶圆的工艺流程
- 基片制备
- 工艺结果依赖性
- 测量和工艺控制

张 源 女士，专家级讲师

张源，1999 年北航材料学硕士毕业后，入职华为，一直从事先进材料及工艺的创新研究。2000~2011 年，曾做为首任 leader 带领创建 PCB、SiP 封装工艺技术业务及团队，并曾任电子材料研发团队的技术首席，开发过多项行业领先技术；期间曾任 IPC 协会 7-31bCN 中国区委员会首任主席，组织 610CN 等标准开发。2011~2020 年曾任 网络及光电板级工程领域的首席规划师，规划并参加开发多款领先全球的关键部件及技术。2020 年至今，出于对行业的热爱，持续板级和封装工程领域的探索，做为个人讲师为行业服务。

演讲摘要：随着数据需求量的不断增加，需要处理器、交换等核心芯片的性能不断提升，而半导体纳米工艺的步伐渐缓，使得封装功耗、物理尺寸、IO 速率不断挑战工程极限。相对电互连，光互连本身具备大带宽、长距传输等优势，而硅光的产业化，更加推动了“光进铜退”的演进，使得光互连进封装（CPO）、进单板（NPO）成为了行业热点。

本文将概要介绍对 CPO/NPO/LPO 的理解，分析其价值及潜在应用场景。阐述行业主流企业 CPO 的研究历程及趋势，剖解其中的关键技术。分析说明光电合封的产业链挑战，以及标准状况。

樊学军 博士，美国拉玛尔大学 教授

樊学军是德克萨斯大学的董事教授，也是德克萨斯州博蒙特市拉玛尔大学的玛丽·安和劳伦斯·E·福斯特教席教授。樊学军博士是 IEEE Fellow 和 IEEE 杰出讲师。他于 2017 年获得杰出持续技术贡献奖，并于 2011 年获得 IEEE 电子封装协会的杰出技术成就奖。樊学军博士是异构集成路线图建模与仿真委员会的联合主席。

演讲摘要：随着高性能半导体的需求不断增加，采用 3D 单片和 2.5D/3D 先进封装技术的异构集成能够显著提高系统性能。因此，电迁移（EM）诱发的微凸块和再分布线（RDL）失效已经成为人们关注的焦点。此外，焦耳加热诱发的热迁移（TM）与电迁移相结合，正在成为微/纳米电子未来的一大潜在风险。在这次演讲中，我将在全耦合建模的基础上，介绍由电迁移（EM）所致失效的设计规则和加速测试的一些一般准则。多年来，现有的 EM 理论只能部分预测或解释实验中的复杂现象。最近，我们在耦合理论的框架下梳理出许多不正确的模型和假设。此外，考虑到多尺度效应，我们用分子动力学模拟确定了关键的微观参数，进而建立了一个完整、自洽的电迁移多物理场耦合模型。为验证模型，我们进一步进行了全面的 EM 测试，并收集了一致的测试数据。理论和数值结果完全再现了实验中的各种现象，包括热迁移的影响。随后，我们采用经过验证的理论为设计规则和加速因子提供了新视角，以防止 EM 诱发的失效。

王启东 博士，中国科学院微电子研究所 系统封装与集成研发中心主任

王启东博士，中国科学院微电子研究所研究员，系统封装与集成研发中心主任。东南大学电子科学与技术系工学学士，英国诺丁汉大学通信与计算机科学硕士，中国科学院大学微电子与固体电子学工学博士。2009 年加入中国科学院微电子研究所，2015-2016 年斯坦福大学访问学者。作为项目与课题负责人承担多项 02 国家重大专项、中科院先导专项、自然基金国际重点合作项目、多地地方重点技术合作项目等。主要研究方向为三维异质集成技术，在 Nature、TAP、AWPL、Phys. Rev. A、JINST、Microelectronics Reliability、MOTL、TNS 等发表文章 60 余篇，申请中国发明专利 76 项，获北京市科技进步奖二等奖 1 项，中国科学院科技促进发展奖 1 项。

口头报告分布

星期五, 8 月 11 日, 10:00-20:30

<table>
<tr><th colspan="8">并行会议</th></tr>
<tr><th></th><th>会场 1</th><th>会场 2</th><th>会场 3</th><th>会场 4</th><th>会场 5</th><th>会场 6</th><th>会场 7</th></tr>
<tr><td>10:00-11:45</td><td>口头报告 1
专题 1</td><td>口头报告 2
专题 2</td><td>口头报告 3
专题 3</td><td>口头报告 4
专题 4</td><td>口头报告 5
专题 6</td><td>口头报告 6
专题 8&9</td><td>口头报告 7
专题 7</td></tr>
<tr><td>主 席</td><td>王启东</td><td>龙 旭</td><td>杨道国</td><td>王晨曦</td><td>谢 斌</td><td>张建华</td><td>叶怀宇</td></tr>
<tr><td>10:00-10:30
特邀报告</td><td>吴政达</td><td>张国平</td><td>刘子玉</td><td>王 谦</td><td rowspan="2">46, 70, 91,
104, 185, 198,
210</td><td>陈维恕</td><td>樊海波</td></tr>
<tr><td>10:30-11:45
口头报告</td><td>23, 54, 55,
87, 125</td><td>21, 34,
35, 78</td><td>22, 24, 28,
42, 45</td><td>119, 149, 189,
190, 200</td><td>138, 151, 179,
279, 403</td><td>247, 387, 624
张 靖
特邀报告</td></tr>
<tr><td>11:45-12:15</td><td colspan="7">张贴报告展出&茶歇</td></tr>
<tr><td>12:15-14:00</td><td>口头报告 8
专题 1</td><td>口头报告 9
专题 2</td><td>口头报告 10
专题 3</td><td>口头报告 11
专题 4</td><td>口头报告 12
专题 6</td><td>口头报告 13
专题 9&10</td><td>口头报告 14
专题 7</td></tr>
<tr><td>主 席</td><td>马盛林</td><td>刘志权</td><td>靖向萌</td><td>刘影夏</td><td>杨晓锋</td><td>尚金堂</td><td>梁红伟</td></tr>
<tr><td>12:15-12:45
特邀报告</td><td>王 玮</td><td>达 宁</td><td>田 忠</td><td rowspan="2">202, 204,220,
221, 301, 319,
417</td><td rowspan="2">264, 292, 307,
320, 326, 386,
420</td><td>陈光雄</td><td>Chuantong CHEN</td></tr>
<tr><td>12:45-14:00
口头报告</td><td>216, 260, 282,
360, 501</td><td>97, 113,130,
133, 206</td><td>57, 69, 79,
94, 117</td><td>64, 98, 122,
134, 146</td><td>323, 553, 621
王 宾
特邀报告</td></tr>
</table>

14:00-15:30	午 餐						
15:30-17:45	口头报告 15 专题 1&5	口头报告 16 专题 2	口头报告 17 专题 3	口头报告 18 专题 4	口头报告 19 专题 6	口头报告 20 专题 10	口头报告 21 专题 2
主 席	王 玮	吴蕴雯	杭 弢	刘子玉	谢 斌	于大全	李宇杰
15:30-16:00 **特邀报告**	蔡琳玲	韩 政	148, 153,186, 240,290, 293, 311, 341, 350	龚 里	421, 467, 472, 514, 526, 528, 533, 598, 643	阮文彪	梅云辉
16:00-17:45 **口头报告**	姚大平 特邀报告	234, 241, 246, 263, 265, 277, 327		424, 425,441, 450, 451,457, 463		233, 274, 276, 284, 354, 382, 460	482, 517, 536, 540, 544, 586, 590
	陈 云 特邀报告						
	513，604，147						
17:45--18:15	张贴报告展出&茶歇						
18:15--20:30	口头报告 22 专题 1&5	口头报告 23 专题 2	口头报告 24 专题 3	口头报告 25 专题 4	口头报告 26 专题 6&7	口头报告 27 专题 10	口头报告 28 专题 2&3
主 席	刘 胜	高丽茵	刘丰满	张 昱	鲁 敏	田艳红	李财富
18:15--20:30 **口头报告**	Richard RAO 特邀报告	328, 329, 333, 338, 351, 367, 388, 432,437	400, 406, 408, 512, 585, 626, 664, 684, 695	471, 473, 522, 525, 599, 610, 660, 669	671, 694, 701, 709, 724, 731, 736, 443, 452	计红军 特邀报告	629, 646, 722, 440, 442, 717, 726, 730
	238, 275, 324, 435, 490					618, 662, 677, 737	

张贴报告分布

<table>
<tr><th colspan="14">星期五, 8 月 11 日, 11:45-12:15 / 17:45-18:15</th></tr>
<tr><th colspan="2">1 区</th><th colspan="2">2 区</th><th colspan="2">3 区</th><th colspan="2">4 区</th><th colspan="2">5 区</th><th>6 区</th><th colspan="2">7 区</th></tr>
<tr><td colspan="2">专题 1
先进封装

专题 2
封装材料与工艺</td><td colspan="2">专题 3
封装设计、建模与仿真

专题 4
互联技术</td><td colspan="2">专题 5
先进制造技术与设备

专题 6
质量与可靠性</td><td colspan="2">专题 7
功率电子与新能源及新型电力系统

专题 8
光电器件与封装</td><td colspan="2">专题 9
微机电封装

专题 10
新兴领域封装与面向人工智能的电子技术应用</td><td>专题 2
封装材料与工艺</td><td colspan="2">专题 1
先进封装

专题 2
封装材料与工艺</td></tr>
<tr><td>255, 303, 322, 361, 449, 454, 492, 515</td><td>4, 44, 67, 88, 92, 129, 163, 227</td><td>10, 56, 135, 140, 142, 150, 222, 224</td><td>33, 90, 401, 462, 551, 659, 704, 706</td><td>195, 209, 219, 237, 262, 280, 287, 296</td><td>6, 12, 32, 37, 48, 63, 72, 73</td><td>11, 76, 80, 121, 235, 244, 332, 357</td><td>20, 89, 131, 249, 251, 306, 316, 317</td><td>384, 465, 582, 708, 728</td><td>5, 15, 167, 191, 225, 429, 487, 510, 511, 587, 592</td><td>228, 229, 231, 253, 295, 304, 308, 321, 335, 353, 364, 399, 404, 407, 413, 439</td><td>549, 559, 563, 603, 651, 698, 741</td><td>504, 519, 529, 613, 614, 687, 688, 689, 690</td></tr>
<tr><th colspan="14">星期五, 8 月 11 日, 11:45-12:15 / 17:45-18:15</th></tr>
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<tr><td colspan="2">专题 3
封装设计、建模与仿真

专题 4
互联技术</td><td colspan="2">专题 5
先进制造技术与设备

专题 6
质量与可靠性</td><td colspan="2">专题 7
功率电子与新能源及新型电力系统

专题 8
光电器件与封装</td><td colspan="2">专题 6
质量与可靠性</td><td colspan="3">专题 2
封装材料与工艺

专题 3
封装设计、建模与仿真

专题 6
质量与可靠性</td><td>专题 6
质量与可靠性</td><td rowspan="2"></td></tr>
<tr><td>248, 346, 398, 405, 438, 448, 481, 530, 570, 573, 639</td><td>707, 711 712, 713, 718</td><td>325, 391, 392, 561, 627, 665, 679, 681</td><td>74, 81, 103, 124, 145, 152, 173, 194</td><td>446, 566, 628, 680, 693, 700, 715, 723, 746</td><td>380, 602, 620, 729,</td><td colspan="2">196, 217, 250, 252, 267, 269, 352, 355, 362, 365, 369, 394, 395, 396, 412, 415</td><td>703, 721, 742, 744, 747</td><td>655, 656, 685, 714</td><td>645, 653, 657, 696, 702, 27</td><td>418, 436, 447, 455, 456, 475, 503, 527, 548, 550, 555, 558, 581, 595, 607, 632</td></tr>
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专题报告人简介

吴政达 博士，三星电子总监

吴政达博士目前于韩国三星电子半导体业务部门先进封装（AVP）业务团队的 BD Team 担任 Director 一职。加入三星电子之前，吴博士于成都奕斯伟系统集成电路有限公司服务，担任首席技术官（CTO）。此前，他也曾于中芯长电及台积电等公司担任重要职务。他于英国牛津大学（Oxford University）获得无机化学博士学位（2014），并分别于中国台湾大学（2006）及中兴大学获得化学工程学硕士及学士学位（2004）。 因为在半导体先进封装的贡献，吴博士也获颁了包括 2018 年江苏省双创人才、2019 年无锡市太湖人才、2021 年成都高新金熊猫人才 C 类、SEMICON China 中国国际半导体技术大会（CSTIC 2022）优秀年轻工程师一等奖等许多荣誉。 吴博士拥有许多著作，其中包含了 14 篇期刊论文和会议论文，总引用次数达 660 次以上、H-index 为 11；此外，他还获得 144 篇中国专利及 40 篇美国专利。

演讲摘要：随着移动、物联网、人工智能、大数据和汽车应用对计算性能的需求不断增长，由于摩尔定律和计算能力解决方案的放缓，对新解决方案的需求也在增长。芯片和先进封装是实现 HPC 和 AI 系统更高带宽和密度的关键平台。本报告将讨论先进封装如何实现下一代计算和通信。

王 玮 教授，北京大学

王玮，2005 年于清华大学航天航空学院获博士学位，导师过增元院士，之后加入北京大学信息科学技术学院和微米/纳米加工技术国家级重点实验室，现任微米纳米加工技术全国重点实验室主任、北京大学集成电路学院副院长、先进技术研究院副院长（挂职），是微米/纳米加工技术国家级科技创新团队学术带头人、入选了国家卓越青年基金项目。主要开展微机电系统、聚合物微纳加工方法、临床微纳系统相关研究，发表 SCI 检索期刊论文 100 余篇，领域顶级国际会议 50 余篇，授权、申请发明专利及软件著作权 50 余项，包括美国专利 3 项。担任微机电系统领域顶级国际会议 IEEE MEMS ‘2015、‘2016、Transducers ‘2019 的执行技术委员会委员，微纳流体前沿国际会议’2015 共同主席；担任多个应用中心、重点实验室学术委员会主任或委员；担任 Microfluidics and Nanofluidics、Microsystems& Nanoengineering 等多个国际、国内期刊的副主编、编辑等。

演讲摘要：针对 Chiplet 先进封装中高密度互连的需求，开展亚微米精度下的芯粒埋置重构晶圆工艺研究，低损伤高平整度的聚合物平坦化工艺研究，以及多应用场景的高密度硅基扇出布线工艺研究，突破了超薄晶圆（<50 μm）的低应力减薄、高精度（±2 μm）无损化切割问题，亚微米精度（<0.5 μm）下的芯粒埋置问题，超低孔隙率（>95%）的高深宽比埋置缝隙聚合物填充问题，超低 TTV（<1 μm）的重构晶圆表面平坦化问题以及多层高密度的互连布线问题，实现了芯粒埋置后的多层 2 μm/2 μm 线宽/线距硅基扇出布线工艺技术，有望应用于 Chiplet 先进封装技术。

蔡琳玲 女士，赛默飞世尔科技（中国）有限公司业务拓展经理

蔡琳玲，拥有 10 多年的电镜技术支持的从业经验，具有坚实的显微镜理论基础以及丰富的实际应用经验，对于电镜产品如何助力于逻辑、存储、化合物半导体、封装以及面板类产品的研发以及良率提升有着持续和深入的研究，对于半导体工业各类样品的的失效分析方法都非常熟悉。基于丰富的应用经验，可以为不同行业的客户提供相适应的电镜解决方案。

演讲摘要：源于更薄更小集成度更高的 IC 产品的需求，先进封装的复杂性与日俱增。随之而来的就是工艺挑战和缺陷分析的复杂性。为了解决这些缺陷问题，从而提高良率并解决客退问题，就需要更高效的失效

分析手段来定位和分析缺陷。赛默飞提供了完整的电性失效分析（EFA）到物性失效分析（PFA）的失效分析解决方案。热定位成像是被市场认可的锁定失效点的无损检测技术。而双束电镜可以高效精确的加工到样品内部的缺陷并通过 SEM 进行高分辨的观察解析，还可以以纳米级精度对于局部区域进行 3D 重构，精准分析失效和工艺问题。此报告重点分享了赛默飞的热定位成像设备、双束电镜以及 SEM 电镜设备在先进封装行业的失效分析应用案例。

姚大平 博士，江苏中科智芯集成科技有限公司董事长、总经理

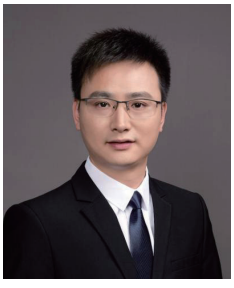
姚大平博士是江苏中科智芯集成科技有限公司的创始人，目前担任公司董事长兼总经理。中科智芯公司成立于 2018 年 3 月，落地在江苏徐州经济技术开发区。姚大平博士于 2017 年 6 月回国，入职华进半导体封装先导技术研发中心有限公司，2017 年受聘为江苏省产业研究院集萃（JITRI）研究员。在华进半导体工作期间，致力于多项先进封装先导技术的研发和应用，其中主要集中在开发与完善晶圆级扇出型封装技术路线、和实施该技术的产业化方案。在回国之前，姚博士任职于美国应用材料公司二十多年，一直从事与集成电路芯片制造相关的工艺制程、工艺集成和工艺设备的研发和产业化工作。姚大平毕业于美国伊利偌大学，获得材料科学与工程博士学位。

演讲摘要：新型先进封装技术，从平面多芯片扇出到三位立体集成相关的异构集成，成为未来业界发展的方向，由于其设计与制作的灵活性与高可靠性，应用场景日益拓展。由各种工艺的重布线、转接板、镶嵌导电桥等信号互连技术使得来自不同制造技术代、不同功能的多颗芯片、甚至模块可以混合封装成一体器件。三维堆叠系统集成技术基于异构混合键合与制作技术促进多芯片系统异构集成受到广泛重视，一致认为是实现超越单一片上系统（SoC）性价比的更优方案。

Richard RAO 博士，美国迈威尔科技资深首席工程师

Richard RAO 博士目前是 Marvell 的资深首席工程师，也是 IEEE 的高级成员。在加入 Marvell 之前，他是 Microsemi（Microchip）Corp.的研究员和 Ericsson Inc.的顾问工程师，他的职责包括开发先进电路、封装和芯片倒封装交互的可靠性流程设计。Richard RAO 博士是 IEEE-EPS（电子封装协会）可靠性技术委员会主席，并共同主持了 IEEE 异构集成路线图的可靠性路线图。同时，还是 IEEE-REPP（电子和光子学封装可靠性）研讨会的总主席和技术项目主席，并担任 IEEE-IRPS（国际可靠性物理研讨会）的技术委员会主席。

Richard RAO 博士，获取了中国科学技术大学固体材料力学博士学位，美国西北大学博士后研究员，研究方向为先进集成电路可靠性失效机理。在加入 Marvell 之前，曾在学术界和工业界担任可靠性物理和工程的高级技术职位。曾任中国科学技术大学副教授、新加坡国家科学技术委员会研究员。



张国平 教授，深圳先进电子材料国际创新研究院，中国科学院深圳先进技术研究院研究员

张国平，男，汉族，中共党员，研究员，博士生导师，“国家高层次人才特殊支持计划”青年拔尖人才，广东省“特支计划”领军人才，IEEE 高级会员、ICEPT 技术委员会委员、中科院青年创新促进会会员。现任中科院深圳先进技术研究院材料所副所长，深圳先进电子材料国际创新研究院副院长，集成电路材料全国重点实验室副主任。他长期从事集成电路先进封装材料领域研究工作，聚焦晶圆级封装关键材料的研发及应用，获深圳市科技进步奖二等奖。先后承担参与国家、省、市等重点科研任务 10 余项，发表 SCI 和 EI 收录论文 100 余篇，申请专利 60 余件，获得授权专利 20 件/国际 PCT 专利 2 件，实现专利转移转化 5 件。创立深圳市化讯半导体材料有限公司。

演讲摘要：随着摩尔定律趋缓，加速部署先进封装技术以满足高端芯片在集成化、多功能化和低成本方面的需求势在必行。深圳先进电子材料国际创新研究院致力于先进电子材料的核心技术突破、技术创新引领，目标建成国际领先、“无可替代”的平台。凭借 10 多年的研发投入和技术积累，在集成电路先进封装关键材料方面能够提供系统解决方案。特别是，研究团队所开发的耐高温临时键合材料已广泛应用于晶圆级封装、2.5/3D 封装和异构集成等先进封装领域。本次演讲主要介绍我们团队最近开发的耐高温临时键合/解键合材料（WLP TB5160/WLP LB601），该材料具有优异的耐腐蚀性、耐温可达 400° C、满足室温键合的高产能要求、与激光/机械剥离法兼容等优点，适用于半导体行业的高温和高应力应用。

达 宁 博士，肖特玻璃科技（苏州）有限公司中国资深运营经理和半导体业务负责人

达宁博士毕业于德国埃尔朗根-纽伦堡大学。他在玻璃、玻璃陶瓷和其他脆性材料领域拥有近 20 年的经验。他于 2013 年加入肖特玻璃，一直深入参与玻璃材料在消费电子和半导体行业的技术研发和应用。目前主要负责肖特玻璃晶圆及相关半导体技术产品的生产运营，以及在中国市场的推广应用。发表学术论文 30 余篇，申请玻璃材料及其应用 PCT 专利 10 余项。

演讲摘要：在后摩尔时代，随着小芯片技术的发展，集成电路行业对芯片的类型、数量、高密度和集成度提出了越来越高的要求。作为一种古老的材料，玻璃以其优异的光学性能、稳定的耐化学性和耐热性以及可定制的膨胀系数和厚度逐渐受到小芯片技术的青睐。肖特根据全球市场的需求，不断开发各种性能的玻璃材料，并制造所需规格的玻璃晶片、载板或 TGV，以满足当前集成电路开发的需求。本次演讲主要介绍肖特可以提供大规模量产的玻璃晶圆和基板材料，厚度范围从 0.03 到 20mm 或以上。此外，翘曲、厚度公差和 TTV 都受到严格控制。根据应用，玻璃晶片可根据要求提供范围从 3.2x10-6 到 9.4x10-6/ºC 的各种热膨胀系数（CTE）。演讲还对影响小芯片工艺的玻璃材料的特性和性能进行了深度的讲解，以助力小芯片行业的发展。

韩 政 先生，JSR 上海公司的销售部高级经理

韩政，JSR 上海公司的销售部高级经理。目前的致力于为 WLP/PLP 和 PCB 行业的下一代先进封装的发展。他将介绍用于高级封装的电镀光刻胶和光成像电介质的发展现状和路线图。此外，他还将介绍用于 PCB 行业的新型低 Df 聚合物。

演讲摘要：本次演讲内容主要包含对于先进封装工艺中使用到的电镀光刻材料的介绍。随着先进封装技术的不断向前发展，RDL 工艺和铜凸块工艺的技术难度越来越高，从而对电镀光刻胶的技术能力也提出了更高的要求。性能优异的电镀光刻胶可以有效解决先进封装电镀工艺中的一些难点。可成像绝缘膜材料一直是先进封装中的重要材料，低残余应力、低收缩、低介电损耗和良好的光刻性能也一直是业内关注的重点方向。CCL 业界在开发高速高频材料时，往往需要引入新型低 Df 聚合物。合适的材料能使开发事半功倍。演讲描述：随着先进封装技术的发展， RDL 的重要性越来越大。先进封装中的 RDL 不仅适用于制作 bond pad 或将互连区域扩展到芯片之外，还适用于高密度芯片之间的连接。此外，先进封装需要高铜凸块来制造封装上封装（PoP）结构。我们为 RDL 和 PoP 开发了先进封装所需的新型电镀光刻胶和介电材料。光刻胶（PR）在溅射铜上表现出优异的耐化学性、良好的涂层性能和高高宽比的良好光刻性能。我们的光成像电介质（PID）表现出低残余应力、低收缩、低介电损耗和良好的光刻性能。此外，我们一直在为 PCB 行业开发新型低 Df 聚合物，以进一步促进不断发展的先进封装技术。

刘子玉 博士，复旦大学教授

刘子玉，复旦大学微电子学院教授，硕士生导师。中国香港城市大学电子工程系博士后，清华大学微电子所博士，吉林大学材料科学与工程学院本科。从事先进封装、三维集成等方向 11 年，主要研究先进封装技术，包括 2.5D/3D 集成、晶圆级封装、系统级封装的设计、模型、工艺、机械/热/电仿真等，特别是在高密度互连键合技术、硅通孔技术、三维无源器件工艺、模型及仿真等方面进行了诸多创新性探索。目前在国内外顶级封装会议（ECTC、ICEPT 等）、顶级封装期刊（TED 等）发表学术论文 50 多篇，申请/授权封装方面相关专利 22 项，在研的省部级以上的项目 3 项，横向项目 1 项，参与 1 项国家重大专项 02 专项，并与多家国内知名封装企业保持合作关系，如华为、通富、华进半导体等。

王 谦 博士，清华大学集成电路学院副教授

王谦 2001 年 1 月于清华大学获得博士学位，先后在东京大学先端科技研究中心、日本物质材料研究机构、韩国三星综合技术研究院、三星半导体中国研究开发有限公司等研究机构进行先进封装互连技术及可靠性、MEMS 封装与测试技术、微系统封装及可靠性分析的研究工作。2010 年 3 月开始在清华大学工作。研究方向主要包括：系统级封装、MEMS 封装、晶圆级封装、三维集成、芯粒集成、异质异构集成等先进互连与封装技术、纳米互连与集成技术及封装可靠性与失效分析等。

演讲摘要：混合键合是应用于 Chiplet 集成和数据密集型应用（如数据中心、高性能计算（HPC）和人工智能（AI））的超高密度互连关键技术。通常，它可以通过芯片到芯片（C2C）、晶圆到晶圆（W2W）和芯片到晶圆（C2W）的混合键合来实现。考虑到芯片产能问题，C2C 混合键合将不会应用于大规模量产。W2W 混合键合也由于相似芯片尺寸和良率的问题而受到限制。C2W 混合键合可以灵活地组装不同尺寸的芯片，因此适合 Chiplet 集成，将成为主流。然而 C2W 混合键合工艺复杂并面临若干挑战，诸如由于切单颗芯片而产生的颗粒和污染物问题、更高精度拾取和放置的要求、Cu/电介质表面形貌的控制、金属焊盘凹陷和键合表面平坦化的 CMP 工艺要求。由于上述严格的工艺要求，导致了 C2W 混合键合的工艺窗口较窄、产能有限。

为了解决上述问题，缩短 C2W 混合键合时间和退火工艺时间，以提高键合产能，我们提出了一种用于 Chiplet 集成的 C2W 混合键合新方案：利用突起的 Cu 焊盘在 200℃的低温和 30MPa 的键合压力下实现 Cu/SiO2 混合键合，键合时间缩短至 5 分钟，并在每个芯粒混合键合到晶圆上之后，将整个圆片在 200℃的温度下退火 30 分钟。传统的 Cu/SiO2 混合键合的键合机理是首先将 SiO2 预键合，然后通过键合后的退火工艺使 Cu 焊盘膨胀，进而实现键合互连。相比之下，本研究在整个 Cu/SiO2 混合键合过程中，首先将突起的 Cu 焊盘连接，并通过温度和压力将其压平，从而放宽了对 CMP 和表面处理工艺的严格要求，也减少了键合后的退火时间和温度。键合时间和温度的降低有助于提高 C2W 混合键合的产能。本文阐述的混合键合方案可以为面向 Chiplet 集成的低温窄节距 C2W 混合键合提供新的思路。

龚 里 博士，苏斯贸易（上海）有限公司总经理

龚里博士就学于德国埃尔朗根-纽伦堡大学，获材料学硕士。此后加入德国夫琅霍夫集成电路研究所。工作的领域是半导体生产工艺技术和测量方法。在专业杂志和国际会议上发表了 20 多篇学术论文。获 Erlangen-Nuernberg 大学电子工程学博士学位。在从事了多年教学科研工作后，于 1994 年底加入 SUSS MicroTec 公司。从 2001 年至今任 SUSS 中国公司总经理。在半导体工艺和设备领域里积累了丰富的经验。

演讲摘要：三维封装，特别在 14 纳米以下受限制的情况下，成为了特别重要的技术。用它可以用 14 纳米技术生产的芯片通过三维的堆叠达到更高的集成度。这样的工艺需要非常好的对准精度和成品率。苏斯作为这个领域里领先的设备公司投入了大量的资源。本文介绍我们在这方面取得的结果。

陈 云 先生，盛美半导体设备（上海）股份有限公司销售经理

陈云，本科学历，2014 年-2018 年就职于华润上华科技有限公司，负责前道 track 工艺调试、优化，2018 年加入盛美上海至今，先后负责先进封装湿法设备工艺研发及调试、先进封装湿法及电镀设备技术销售等工作，目前是盛美上海先进封装及第三代半导体市场销售负责人，在前道制程、先进封装领域拥有 8 年以上半导体工艺及技术销售经验。

演讲摘要：在芯片堆叠密度不断增长及多芯片整合的需求下，HDFO、2.5D/3D 等更先进的晶圆级封装技术在国内先后推出，相关设备的要求不断提高。盛美上海已成功解决大翘曲晶圆在传输和工艺夹持中的难题，成功开发了高速电镀、特殊控制搅拌桨、六元合金弹性触点等先进单片式电镀技术/专利，在提高电镀沉积速率的同时较好的控制了电镀均匀性，银含量等参数，保证品质的前提下有效帮助客户提升产能。此外，盛美上海还提供匀胶、显影、去胶、腐蚀及清洗等全套先进封装湿法设备解决方案。

樊海波 博士，中国香港安世半导体高级首席工程师

樊海波博士，安世半导体中国香港公司封装研发-先进材料技术与建模高级首席工程师。他在中国香港科技大学（HKUST）获得博士学位，后在 HKUST、飞利浦 LED 照明全球研发中心、NXP Hong Kong (China)和 Nexperia Hong Kong (China)工作，拥有 20 多年的仿真经验，以及 15 年的设计和可靠性行业经验；他撰写或合著了 50 多篇同行评议的技术出版物，出版了 2 本书和 3 本书的章节。

演讲摘要：在保持尽可能高的可靠性的同时，设计具有高效率和高功率密度性能的功率封装是一项挑战。然而，功率封装存在许多可靠性问题，如分层、芯片裂纹和焊料裂纹等。需要进行设计优化以尽可能降低风险。同时，客户对产品的要求也更加严格，以满足汽车产品应用的高要求。因此，充分了解引起这些问题的因素有助于推动设计和工艺优化，从而实现更稳健的封装设计。

在汽车电子、便携式电力电子和大功率模块中，数值建模可以作为虚拟原型，预测装配过程中的问题，并进行广泛的可靠性测试，以优化设计和工艺。仿真驱动的制造设计方法可直接为早期风险评估提供可制造性见解，从而最大限度地降低分层、芯片裂纹、封装裂纹、焊料疲劳等风险，实现设计和工艺优化，帮助产品尽早、更快地推向市场。

在本次演讲中，将讨论从芯片级到板级的设计和可靠性方面的挑战，并通过几个案例展示如何通过仿真驱动设计以实现稳健的功率封装设计。此外，还将基于机器学习与有限元分析相结合的方法，讨论人工智能仿真在半导体工艺和可靠性方面的应用。

张 靖 博士，贺利氏电子中国区研发总监

张靖博士，贺利氏电子中国区研发总监。张靖博士毕业于荷兰代尔夫特理工大学，专注于高功率电子封装工艺以及可靠性的研究。2017 年，张靖博士加入德国贺利氏，研究领域主要集中在第三代半导体器件先进封装技术与可靠性评估方面。迄今，张靖博士领导或参与的国内国际研发项目超过 30 项，经费超过 9000 万元，作为第一负责人主持的项目经费超过 4000 万元。多项项目成果已被应用到相关产业当中，包括新能源汽车，高铁，半导体照明等。迄今已发表论文超过 20 篇；学术专著 1 篇；受邀国际学术会议大会报告 9 次。张靖博士任 IEEE 封装学会（EPS）荷比卢分会首任创会主席，国际宽禁带半导体技术路线图委员会（ITRW）执行秘书，并任封装分会委员。张靖博士同时担任上海碳化硅功率器件工程技术研究中心技术委员会委员，第三代半导体创新产业联盟青年委员会委员，中国第三代半导体路线图委员会封装分会委员，纳米烧结材料标准制定委员会成员。张靖博士现为复旦大学校外硕士研究生导师。

演讲摘要：随着碳化硅功率器件在许多领域的应用明显加速，以实现更高的功率密度和开关频率，市场亟

需合适的封装材料和解决方案来最大限度地提升此类器件的优势。封装的一项关键工序做芯片上表面的互联。然而，对于碳化硅模块来说，传统铝线键合线在载流能力，导热能力和可靠性方面已经逼近其极限。另一方面，基于 Die top system（DTS）技术的铜线键合可实现牢固可靠的互联，并且提供更高的电流能力和可靠性。本场演讲将详细介绍 DTS 技术此外，以展示该解决方案如何最大限度地提升热，电性能和宽禁带器件的可靠性，以及最多能提高至什么水平。

Chuantong CHEN 教授，日本大阪大学

Chuantong CHEN，分别于 2012 年和 2015 年获得日本名古屋工业大学机械工程专业硕士和博士学位。2016 年至 2019 年，他在日本大阪大学科学与工业研究所担任助理教授。2020 年起，他成为大阪大学副教授。他的研究兴趣包括无铅焊接、银烧结接合、纳米接合、三维封装和电力电子封装。陈教授曾获得一些奖项和荣誉，包括 2023 年 IEEE ICEP 杰出技术论文奖和 2019 年 IEEE CPMT 日本分会青年奖。他在上述领域发表了包括《IEEE T Power Electr》、《Acta Mater》、《Scripta Mater》、《Appl Phys Lett》在内的 100 多篇期刊论文和约 70 篇会议论文。他还申请并获得了 15 项日本和国际专利，其中包括 3 项美国专利。陈教授 2020 年起担任 IEEE ICEPT 技术委员会委员，2020 年起担任日本电子封装学会关西分会委员，2018 年起担任日本第三代半导体封装基板材料、互连、热传导评估系统和设备国际标准委员会委员。

演讲摘要：SiC 和 GaN 具有比 Si 更宽的带隙，并且能够承受高温和高频工作。碳化硅和氮化镓可减少功率损耗，全面缩小电力电气设备的尺寸。由于功率较大，SiC 功率模块的工作温度可达到 250℃以上。银（Ag）烧结连接正逐渐成为电力电子领域芯片连接的重要互连技术。与传统的焊接或导电胶连接方式相比，银（Ag）烧结连接具有卓越的加工能力、耐高温性和长期的耐用性。大量研究表明，在温和的烧结条件下（无压、低温和大气烧结），银烧结膏体能够在 DBC 基板上实现稳健可靠的芯片连接。然而，银烧结连接也面临着一些巨大的问题，例如，价格昂贵（尤其是纳米银浆）、SiC 之间的 CTE（热膨胀系数）不匹配导致的界面应力过大和可靠性问题，以及高温热迁移导致的烧结银浆微观结构粗化问题。在本报告中，我们将概述银烧结连接，并提出一些新的芯片连接技术，以实现碳化硅功率模块在高温条件下的低材料成本和高可靠性。针对具有低成本、低 CTE 和高可靠性特性的高温应用，将引入铜烧结连接、银硅复合烧结和银铜复合烧结等贴片技术。此外，还将介绍接合质量和键合机制，以便全面了解银烧结接合以外的碳化硅功率模块。

王 宾 教授，清华大学

王宾，清华大学电机系副研究员，博士生导师，IET FELLOW，石河子大学绿洲学者特聘教授，绿色能源与电力安全北京市国际科技合作中心副主任，IEEE 中国区变电站专委会副主席兼秘书长。长期从事交直流混联电网故障分析与安全防御、基于人工智能的电网健康诊断与因果分析等方向的教学和研究工作。主持中国科协国际科技组织事务专项、国家自然科学基金等纵向项目 18 项，获 2017 国家技术发明二等奖及北京市、陕西省、吉林省、福建省、中国电力科技奖等省部级一等奖 8 项。

演讲摘要：介绍承载高比例新能源的交直流混联电网安全保障需求，技术挑战。分别从输电网、配电网两个层面，介绍了相关的故障分析、故障检测、继电保护、故障测距、智能运维等关键技术。

梅云辉 教授，天津工业大学电气工程学院常务副院长

梅云辉，天津工业大学电气工程学院，教授、博导、电气工程学院常务副院长。长期从事电力电子器件封装与可靠性研究，近年主持国家“优青”，天津市“杰青”，国家基金项目、国防预研项目、“慧眼行动”项目、航空基金、华为、蔚来汽车、汇川技术等企业合作项目近 30 项，参与国家基金重点项目、863 项目等。担任中国电源学会理事、元器件专委会副主任、IEEE Senior Member、《电源学报》编委、天津市电源学会副理事长等。发表学术论文 140 余篇，其中 SCI 论文收录 97 篇，授权发明专利 27 件，曾获 IEEE CPMT Young Award（电子封装学会优秀青年奖）、中国电源学会技术发明奖一等奖（第一完成人）、中国电工技术学会技术发明奖一等奖（第一完成人）、天津市技术发明奖一等奖（第二完成人）、教育部霍英东教育基金高等院校青年科技奖、电工技术—正泰科技奖、IEEE 国际电力电子年会 APEC Best Presentation Award、国家第三代半导体产业技术创新战略联盟(CASA)“特别贡献奖”等。

陈光雄 先生，日月光集团工程资深副总

陈光雄，目前担任日月光中坜厂工程发展中心资深副总经理，领导研发团队在先进封装中不断创新，并推进与客户合作。陈副总在半导体封装制造领域深耕 30 多年，致力于封装技术、MEMS 传感器、晶圆凸块、倒装芯片封装、先进封装以及系统级封装 SiP 解决方案。

陈维恕 博士，夸泰克（广州）新材料有限责任公司副总经理

陈维恕博士 1997/10/1-2002/10/1 任职中国台湾工业技术研究院设备工程师及负责半导体逻辑集成电路设备维护。2002/11/1-2003/10/1 任职中国台湾锌宝科技股份有限公司技术经理负责红光及蓝光 OLED 元器。2003/11/1-2017/10/1 任职中国台湾工业技术研究院研发课长及经理负责建设相关 300mm 工艺。2017/11/1-2019/10/1 任职比思科股份有限公司(韩国)，负责半导体量产前后段干式光刻胶剥除机工艺建置及认证。2019/11/1-2020/10/1 任职山东职业学院铁道供电与电气系正教授，负责电子技术教学与半导体相关课程。2020/10/1 到本公司广州总部就职夸泰克副总经理至今。负责公司高端电子级旋涂化学品材料车间建置及量产产品项目开发。

演讲摘要：用于半导体或显示光学器件的高反射率绝缘层保护膜是由高折射率含金属绝缘层和低折射率含硅绝缘层重复重叠涂覆而成的布拉格反射结构。本文报道了超低折射率自旋玻璃(SOG)封装绝缘层材料的制备工艺、烘烤工艺、表面活性剂配方的优化、空气老化对涂层缺陷的影响以及过滤 SOG 溶液对膜表面微尘的影响。本文报道的 SOG 的最小折射率(n)可低于 1.2@633nm 波长，最佳烘烤工艺为低、中、高温烘烤三步，分别为 80℃/150℃/300℃。表面活性剂的最佳料重比为 1 个基本单位。隔离空气中的水和/或氧气可以消除自旋涂层缺陷。过滤液体后，消除膜表面的细粉尘。目前该材料的 SPC 数据已经达到量产规格。

阮文彪 博士，厦门云天半导体科技有限公司研发总监

阮文彪，中科院博士，电子学与固体电子学专业，现任厦门云天半导体科技有限公司研发部总监，负责玻璃通孔(TGV)、扇出型封装(WL-FO)、晶圆级封装技术、玻璃基高频器件等工艺研发。先后在中芯国际集成电路制造有限公司、中国科学院微电子研究所、北京地太科特技术有限公司任职。2010 年在中科院微电子研究所被聘为副研究员，开展 65 纳米及以下集成电路制造工艺建模和可制造性设计方法学研究，参与和完成多项国家重大专项课题研究。发表文章 10 多篇，申请专利 18 项。

演讲摘要：应用基于先进的集成电路制造工艺的 IPD(集成无源器件)，相比传统的无源器件具有以下优点：体积明显减小，更加轻薄，高性能且一致性更好，成为射频系统小型化、高集成度要求的有效方案。云天

半导体成功开发了国际领先的基于玻璃基的 TGV 制造技术，研究高深宽比 TGV 填充技术，具备多层 RDL 走线设计与工艺实现能力，在此基础上，与 IPD 设计企业紧密合作、协同开发，开发出高性能电感、电容、滤波器、毫米波天线等无源器件，为实现高密度、小型化的高频集成系统奠定技术基础。

计红军 教授，哈尔滨工业大学（深圳）

计红军，1999 至 2008 年在哈尔滨工业大学学习，获工学博士学位，现任哈尔滨工业大学（深圳）材料科学与工程学院教授，长期从事功率超声在微纳连接、先进电子封装互连等领域的基础和应用基础研究。主要研究方向包括超声加工原理与技术（超声辅助材料制备合成、超声金属焊接、超声辅助塑性变形、超声与材料表界面的组织-性能互相作用规律研究等）和先进电子封装互连材料与微纳连接技术（引线键合、芯片键合等）等。相关研究结果在 Scripta Materialia、Ultrasonics Sonochemistry 等国际高水平专业期刊上发表 SCI 论文 70 余篇、国际会议论文 50 余篇，在 ECTC、ICEPT 等电子封装国际会议上做口头报告 40 余次。

演讲摘要：针对高导热/导电、低温连接、高可靠性的先进封装，芯片互连急需进一步降低工艺条件，提升互连质量和稳定性。Cu-Cu 低温互连技术是未来先进封装的核心技术，相较于目前主流应用的 Sn 基软钎料工艺，其能够实现窄间距互连、导电导热能力更强且可靠性更好。本次报告以先进封装中的芯片低温互连技术为背景，介绍应用于先进封装互连的 Cu-Cu 低温互连工艺的最新研究进展及其共性工艺难点。结合课题组的研究成果，着重介绍 Cu-Cu 低温超声焊接工艺和基于纳米材料中间层的 Cu-Cu 低温互连新方法，以及 Ag-Ag 低温互连技术。

口头报告

星期五，8 月 11 日，10:00--20:30

口头报告 1	口头报告 2
地点 会场 1 **专题** 先进封装 **主席** 王启东 博士	**地点** 会场 2 **专题** 封装材料与工艺 **主席** 龙 旭 教授
专题特邀报告 10:00-10:30 **用于未来计算和通信的 Chiplet 和先进封装** *吴政达 博士* 三星电子总监	**专题特邀报告** 10:00-10:30 **耐高温临时键合/解键合材料（WLP TB5160/WLP LB601）** *张国平 教授* 深圳先进电子材料国际创新研究院
23 10:30-10:45 **Technology Development of Wafer-level Ultra-high Density Fan-out (UHD FO) Package** *Dongzhi Fu* Huatian Technology (Kunshan) Electronics Co., Ltd.	21 10:30-10:45 **Reflow Soldering Using Flux-sprayed Solder Preforms** *Fred Fuliang Le* Nexperia HK
54 10:45-11:00 **A High Density QFP With Hybrid Lead** *Chao Ma* NXP semiconductor	34 10:45-11:00 **A Thin Film Metallization Process Development for Silicon Nitride Ceramic Substrates in Power Electronics Packaging** *Xin Chen* School of Materials Science & Engineering Beijing Institute of Technology
55 11:00-11:15 **Deposition Efficiency Study on Wafer Level Gold Plating based on Cyanide-free Electrolyte** *Zhaowei Jia* ACM Research (Shanghai), Inc.	35 11:00-11:15 **Preparation and performance analysis of micro-nano silver powder for solar cells** *Siwei Tang* Central South University
87 11:15-11:30 **Fan-Out Embedded Bridge Solution for Chiplet/HBM Integration** *Mark Liao* PATSD Division, SPIL	78 11:15-11:30 **The Influence of Welding Interfacial Voids on the Thermal Conductivity of Space-borne High-power Electronics** *Le Zhang* China Academy of Space Technology (Xi'an)
125 11:30-11:45 **Electrical Performance Enhancement Solution with FO-EB in HPC Application** *Po Yuan Su* Siliconware Precision Industries Co., Ltd.	

口头报告 3	口头报告 4
地点　会场 3 **专题　封装设计、建与仿真** **主席　杨道国 教授**	**地点　会场 4** **专题　互连技术** **主席　王晨曦 教授**
专题特邀报告 10:00-10:30 **电热力协同仿真优化三维集成关键技术** *刘子玉 博士* 复旦大学	**专题特邀报告** 10:00-10:30 **一种用于小芯片集成的铜/二氧化硅混合键合新策略** *王 谦 博士* 清华大学
22 10:30-10:45 **On-Die Power-Rails Isolation Using Package Loop Inductance** *Vinod Arjun Huddar* Rambus	119 10:30-10:45 **Enabling Low-k Liner in Ultra-high Aspect Ratio TSVs by the Timing of Vacuum Treatment in the Vacuum-assisted Spin-coating Technique** Ziyue Zhang BIT Chongqing Institute of Microelectronics and Microsystems; School of Integrated Circuits and Electronics, BIT
24 10:45-11:00 **Achieving non-underfill SMT process for large size packages by creative package pin map and PCB pad designs** *Hongbin Shi* Huawei Technologies Co., Ltd.	149 10:45-11:00 **Effect of insulating material and structure on the reliability of silicon through hole under thermal stress** *Zongyang Li* Beijing Microelectronics Technology Institute
28 11:00-11:15 **Underfill Flow Numerical Simulation for Achieving Board Level Low Cost and High Reliability of Mobile Devices** *Yiming Jiang* Huawei Technologies Co., Ltd.	189 11:00-11:15 **Selective Wet Etching Technology in 3D NAND Flash Manufacture** *Zihan Zhou* School of Materials Science and Engineering, Shanghai Jiao Tong University
42 11:15-11:30 **Rough Interface Effect on High-Temperature Reliability of TSV for Electronic Packaging** *Weishan Lv* Huazhong University of Science and Technology	190 11:15-11:30 **Anti-oxidation property of nanotwinned copper micro-cone array for low-temperature bonding** *Peixin Chen* Shanghai Jiao Tong University
45 11:30-11:45 **Modeling Methodology for Mechanical Shock Reliability Enhancement Designs of Ultra-Large BGA Packages** *Jianghai Gu* CISCO	200 11:30-11:45 **Study on Low-Temperature Bonding and Reliability of Nano-Twin Copper Micro-Cone Array** *Chongyang Li* Shanghai Jiao Tong University

口头报告 5	口头报告 6
地点 会场 5 专题 质量与可靠性 主席 谢 斌 博士	地点 会场 6 专题 光电器件封装 & 微机电封装 主席 张建华 教授
46 10:00-10:15 **Study on the Application of Auger Electron Spectroscopy in RDL Failure Analysis** *Yanfei Zhao* Wintech-Nano (Suzhou) Co., Ltd.	**专题特邀报告** 10:00-10:30 **半导体光学器件封装用高反射率绝缘薄膜材料的研制** *陈维恕 博士* 夸泰克（广州）新材料有限责任公司副总经理
70 10:15-10:30 **Three-point Bending Test Method Experimental Study for Package Strength and Crack Prediction through Finite Element Analysis** *Minyan Wu* Packaging Technology Development Team, Samsung Semiconductor (China)R&D CO., LTD.	138 10:30-10:45 **In-plane heat transfer enhancement of phosphor layer in transmissive laser-excited white lighting** *Weixian Zhao* Huazhong University of Science and Technology
91 10:30-10:45 **Thermal fatigue behavior of Cu/Co-P/Sn/Co-P/Cu solder joint interface with crystalline/amorphous Co-P coating** *Shuang Liu* Beijing University of Technology	151 10:45-11:00 **Phosphor-in-glass film on AlN substrate for high-luminance white laser Lighting** *Zikang Yu* School of Aerospace Engineering, Huazhong University of Science and Technology
104 10:45-11:00 **Study of the s hear strength behavior in flip chip under thermo mechano electrical coupling and different s older height** *Bin Zhou* Key Laboratory for Microsystems and Microstructure Manufacturing; Harbin Institute of Technology	179 11:00-11:15 **A novel circular position sensitive detector (CPSD) for continuously high-precision rotary angle measurement** *Xiangxu Meng* Institute of Microelectronics of Chinese Academy of Sciences
185 11:00-11:15 **Quantitative analysis of the interface strength of ultra-thin dielectric films based on fan-out packaging** *Zhanxing Sun* Institute of Microelectronics of Chinese Academy of Sciences	279 11:15-11:30 **Simulation Study on Temperature Field of Packaged High Power GaN Laser Diodes** *Hui Liao* University of Shihezi
198 11:15-11:30 **Effects of Porosity on Thermal Resistance Aging at Submicron Silver Interfaces** *Jian Wang* School of Energy and Power Engineering, Shandong University	403 11:30-11:45 **The structural optimization of heterogeneous integration system in display based on thermal reliability analysis** *Sixin Huang* Huawei Technologies Co., Ltd.
210 11:30-11:45 **Studies and Application of A Novel Failure Localization Method for 3D Stacked IC Chips** *Zhang Linhua* Wintech-Nano (Suzhou) Co., Ltd.	

口头报告 7	
地点　会场 7 **专题　功率电子与新能源及新型电力系统** **主席　叶怀宇 教授**	
专题特邀报告 10:00-10:30 **稳健功率封装设计与仿真驱动产品开发** *樊海波 博士* 中国香港安世半导体高级首席工程师	
247 10:30-10:45 **Numerical simulation of bonding wire lift-off of IGBT under power cycling** *Shengjun Zhao* Faculty of Materials and Manufacturing, Beijing University of Technology	
387 10:45-11:00 **A gate driver circuit for crosstalk suppression of SiC MOSFET in half-bridge configuration** *Longnv Li* Tiangong University	
624 11:00-11:15 **Inductor Design for Four-switch Boost/drop Power Supply Module** *Yiying Bao* Microsystem Packaging Research Center, Institute of Microelectronic of Chinese Academy of Sciences	
专题特邀报告 11:15-11:45 **用于碳化硅功率器件的创新封装解决方案** *张 靖 博士* 贺利氏电子中国研发总监	

口头报告 8	口头报告 9
地点 会场 1 专题 先进封装 主席 马盛林 教授	地点 会场 2 专题 封装材料与工艺 主席 刘志权 教授
专题特邀报告 12:15-12:45 **2μm/2μm 线宽/线距多层硅基填埋扇出工艺技术** *王 玮 教授* 北京大学	专题特邀报告 12:15-12:45 **肖特玻璃晶圆和电路板-助力集成电路先进封装** *达 宁 博士* 肖特玻璃科技（苏州）有限公司中国资深运营经理和半导体业务负责人
216 12:45-13:00 **FOStrip® Technique for Low-Cost Fan-Out Package** *I-Hung Lin* Kore Semiconductor Co., Ltd.	97 12:45-13:00 **Selective Laser-induced Etching of Borosilicate Glass in Hydrofluoric Acid** *Yue Zhan* School of Microelectronics, Southeast University, Wuxi
260 13:00-13:15 **Solution to Optimize Warpage performance for 2.5D Fanout Packaging** *Yue Jiang* State Key Laboratory of Mobile Network and Mobile Multimedia Technology, ZTE Corporation, Shenzhen	113 13:00-13:15 **High energy dissipation composite elastomer for application as a thermal interface material through solvent-induced dis-entanglement** *Weijian Wu* Shenzhen Institute of Advanced Electronic Materials
282 13:15-13:30 **Influence of defects in temporary bonding pairs on the effectiveness of UV laser debonding** *Jieyuan Zhang* Shenzhen Institute of Advanced Electronic Materials	130 13:15-13:30 **Effects of silver paste glass additive composition on co-firing behavior of a silver conductor LTCC package** *Zhuofeng Liu* National University of Defense Technology
360 13:30-13:45 **Study on Low Temperature Interconnected nt-Cu/In Solder Joint Interface in System in Package** *Zicheng Sa* Harbin Institute of Technology	133 13:30-13:45 **Copper Low Temperature Co-fired Ceramic: next generation of LTCC for low-cost, high strength and high frequency space applications** *Shicheng Yang* China Aerospace Science and Technology Institute 504
501 13:45-14:00 **Thermal Performance of 2.5D Packaging with the Through Glass Via (TGV) Interposer** *Jin Zhao* Beijing University of Technology	206 13:45-14:00 **Carbazole-grafted Polyimide with Enhanced Adhesion to Smooth Copper** *Zimeng He* Shenzhen Institute of Advanced Technology

口头报告 10		口头报告 11	
地点 会场 3 专题 封装设计、建模与仿真 主席 靖向萌 博士		地点 会场 4 专题 互连技术 主席 刘影夏 教授	
专题特邀报告 **后摩尔时代，系统级封装（SIP）能否成为中国的出路？** *田 忠 教授* 电子科技大学	12:15-12:45	202 **Theoretical analysis and prediction for thermal stress of sintered silver interconnection structure based on modified Suhir's solution** *Jiahui Wei* Faculty of Materials and Manufacturing, Beijing University of Technology	12:15-12:30
57 **Radiated Emissions Prediction of an Electronic Packaging Based on Near-field Scanning** *Di Wang* Zhejiang University	12:45-13:00	204 **Toward next generation interconnection technology: Ag/Cu sinter joining and their innovative application** *Yue Gao* Heraeus Electronics	12:30-12:45
69 **Prediction of Electromagnetic Leakage from Circuits inside Package** *Si-Yao Tang* Zhejiang University	13:00-13:15	220 **Mode I fracture of graphene reinforced Sn-Ag-Cu solder joints** *Jianfeng Wang* Beijing University of Technology	12:45-13:00
79 **Mechanical properties of IGBT module under Temperature shock test considering residual stress** *Rui Wang* NARI-GEIRI Semiconductor Co., Ltd.	13:15-13:30	221 **Thickness effect on shear fracture toughness of sintered silver joints** *Rong Kang* Beijing University of Technology	13:00-13:15
94 **The Effect of Pore Defects on the Interfacial Thermal Resistance of GaN-Diamond Heterostructure** *Chao Yang* School of Energy and Power Engineering, Shandong University	13:30-13:45	301 **A Novel Low-temperature Co-Co Direct Bonding for Future 3D Interconnections** *Xiaoyun Qi* Harbin Institute of Technology	13:15-13:30
117 **Low Modulus Polyimide Coating on Wedge Bond to Improve Wire Bond Robustness in Thermal Cycling** *Ou Dong* Nexperia	13:45-14:00	319 **Low-temperature direct bonding of strengthened glass chips for optical imaging and co-packaged Optics** *Yu Du* Harbin Institute of Technology	13:30-13:45
		417 **A Novel Focused Induction Heating Method For The Interconnection Between High-power Devices And Integrated Circuit Board** *Peng Cui* School of Materials Science and Engineering, Harbin Institute of Technology, Shenzhen	13:45-14:00

口头报告 12	口头报告 13
地点 会场 5 专题 质量与可靠性 主席 杨晓锋 博士	地点 会场 6 专题 微机电封装 & 新兴领域封装与面向人工智能的电子技术应用 主席 尚金堂 教授
264 12:15-12:30 **Study on cracking behavior of sintering silver joints based on cohesive zone model** *Rui Yang* Beijing University of Technology	**专题特邀报告** 12:15-12:45 **车用电子封装及未来发展** *陈光雄 先生* 日月光集团 工程资深副总
292 12:30-12:45 **Development of Low-warpage Bonding Pair by Finite Element Analysis** *Yalin Zeng* Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences	64 12:45-13:00 **Location Identification Method for Soldering Devices of SMT Based on ConvRes-UNet** *Yiqing Yang* Guilin University of Electronic Technology
307 12:45-13:00 **Micro Solder Defect Inspection Using Infrared Sequence and OmniScaleCNN Deep Learning Model** *Ye Jiang* School of Mechanical Science & Engineering, Huazhong University of Science and Technology	98 13:00-13:15 **Welding process expert system based on industrial internet and neural network** *Xiaochuan Xie* GuangZhou Risong Intelligent Technology Holding Co., LTD.
320 13:00-13:15 **A New High-efficient Burn-in Screening Methodology Applied in Integrated Circuits Reliability** *Yalan Sheng* SANECHIPS	122 13:15-13:30 **Structure Optimization Design of Interfacial Failure Resistance for Composite Film in Flexible Electronics** *Hongshi Ruan* College of Mechanical Engineering, Zhejiang University of Technology
326 13:15-13:30 **Failure Analysis for IIH leakage on 7nm FinFET Technology Chip** *Shuanshe Chao* State Key Laboratory of Mobile Network and Mobile Multimedia Technology	134 13:30-13:45 **Conjugated Small Molecule Crystals as A Coupling Layer Between Carbon-based Thermal Interface Materials and Heat Sink** *Daoqing Liu* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology
386 13:30-13:45 **Time Dependent Dielectric Breakdown of 4H-SiC MOSFETs in CMOS technology** *Yaqian Zhang* Delft university of technology	146 13:45-14:00 **High-Performance Thermal Interface Material with A Radial Filler Skeleton** *Jingjing Zhang* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology
420 13:45-14:00 **The prediction of the solder ball crack based on artificial neural network using S parameters** *Huanpeng Wang* Yangtze Delta Region Institute (Huzhou), University of Electronic Science and Technology of China	

口头报告 14	
地点　会场 7 **专题　功率电子与新能源及新型电力系统** **主席　梁红伟 教授**	
专题特邀报告 12:15-12:45 **在高温应用中的 WEB 功率器件的银烧结及超越银烧结连接技术** *Chuantong CHEN 教授* 日本大阪大学	
323 12:45-13:00 **A resonance suppression strategy of LCL-type grid-connected inverter based on compound voltage feedforward** *Haichao Yan* College of Mechanical and Electrical Engineering, Shihezi University	
553 13:00-13:15 **Collaborative Optimization of Multi-energy Complementary System via Game Theory** *Tongqing Song* Shanghai Jiao Tong University	
621 13:15-13:30 **Design Hydro-Solar-Wind Multi-energy Complementary System via Multi-Objective Optimization** *Haotian Tang* Shanghai Jiao Tong University	
专题特邀报告 13:30-14:00 **承载高比例新能源的交直流混联电网故障检测与保护技术** *王 宾 教授* 清华大学	

口头报告 15	口头报告 16
地点　会场 1 **专题　先进封装** **主席　王 玮 教授**	**地点　会场 2** **专题　封装材料与工艺** **主席　吴蕴雯 教授**
专题特邀报告 15:30-16:00 **3D 封装研发及失效分析解决方案** *蔡琳玲 女士* 赛默飞世尔科技（中国）有限公司业务拓展经理	**专题特邀报告** 15:30-16:00 **实现高密度和低损耗先进封装的关键光刻材料** *韩 政 先生* JSR 上海公司的销售部高级经理
专题特邀报告 16:00-16:30 **芯片异构集成封装进展** *姚大平 博士* 江苏中科智芯集成科技有限公司董事长、总经理	234 16:00-16:15 **Copper nanoparticle pastes with organic compounds as anti-oxidative additive for Cu–Cu bonding in air** *Xiaocun Wang* Fudan University
专题特邀报告 16:30-17:00 **先进封装设备技术与提升方案** *陈 云 先生* 盛美半导体设备（上海）股份有限公司销售经理	241 16:15-16:30 **Suppression of Kirkendall Voids at the Interfaces of Sn/nc-Cu Solder Joints** *Xinwei Tian* School of Materials Science and Engineering, Dalian University of Technology
513 17:00-17:15 **Effect of dimension and defects on the flexibility of ultra-thin chips for wearable electronics** *Yan Pan* Shenzhen Institute of Advanced Electronic Materials, SIAT, CAS	246 16:30-16:45 **Microstructure and properties of Sn3.0Ag0.5Cu micro-bumps with nickel-coated graphite and nickel-coated carbon fibers additions** *Yihui Du* Beijing University of Technology
604 17:15-17:30 **Prediction of bonding strength for sintered Ag/DBA joints based on cohesive zone model** *Libo Zhao* Faculty of Materials and Manufacturing, Beijing University of Technology	263 16:45-17:00 **Enhancing properties of low-temperature pressureless Ag sinter-joining by optimizing solvents and hybrid particles** *Yitian Li* School of Mechanical Engineering, Jiangnan University
147 17:30-17:45 **Ablation Behaviour of Photosensitive Materials in Laser Debonding Processes for Advanced Packaging** *Fangcheng Wang* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS	265 17:00-17:15 **Rapid and low temperature Cu particle sintering for power devices with mixing of MOD ink and reductive additives** *Jianbo Xin* School of Material Science and Engineering, Harbin University of Science and Technology
	277 17:15-17:30 **Surface Protecting and Particles Removing after Wafer Sawing for Die-to-wafer Hybrid Bonding** *Hao Wang* School of Microelectronics, Fudan University
	327 17:30-17:45 **First Principle Study of the Adsorption Behavior of 1,2,4-Triazole on Defective Copper Surface** *Pengfei Chang* School of Materials Science and Engineering, Shanghai Jiao Tong University

口头报告 17		口头报告 18	
地点 会场 3 专题 封装设计、建模与仿真 主席 杭 弢 教授		地点 会场 4 专题 互连技术 主席 刘子玉 博士	
148 **A crosstalk mitigation method of DDR5 in large size LGA package** *Keqing Ouyang* State Key Laboratory of Mobile Network and Mobile Multimedia Technology	15:30-15:45	**专题特邀报告** **混合键合技术在三维封装中的应用** *龚 里 博士* 苏斯贸易（上海）有限公司总经理	15:30-16:00
153 **Power Noise Coupling Simulation of DDR4 For FCBGA Packaging** *Zhang Jianguo* Department of Packaging and Testing, ZTE Corporation	15:45-16:00	424 **Effect of ultrasound-assisted Zn content on Cu/Al interconnections in high temperature solders** *Jin Zhou* Chongqing University of Technology	16:00-16:15
186 **Research on the electromigration failure of W interconnects under high-temperature environment** *Yong Wang* Zhejiang University of Technology	16:00-16:15	425 **Modeling and Simulation of a High Bandwidth Conical 3D Monopole Antenna for 3D IC** *Yang Wang* School of Microelectronics, Fudan University	16:15-16:30
240 **A combined experimental and analytical study of residual strains developed in encapsulated structures** *Xiang Li* Institute of Electronic Engineering, China Academy of Engineering Physics	16:15-16:30	441 **Low-temperature Cu/SiC heterogeneous interconnection using Sn-Ag-Ti(La) under high-frequency ultrasound** *Hao Yang* Chongqing University of Technology	16:30-16:45
290 **Simulation and Performance Test of High Bandwidth PCB Based on Multichannel Vertical Interconnection High Frequency Connector** *Miao Wu* Device Technology Department National Optoelectronics Innovation Center	16:30-16:45	450 **Copper electroplating of through silicon vias (TSV) using series of nitrogen-containing heterocyclic compounds** *Ke-Xin Chen* Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences	16:45-17:00
293 **Optimizing Hierarchical 3-D Floorplanning with simulated annealing Algorithm** *Chengyi Liao* Microsystem Packaging Research Center, Institute of Microelectronic of Chinese Academy of Sciences	16:45-17:00	451 **Reliability Study of Two-Step Plasma-Activated Copper-Copper Direct Bonding in Ambient** *Liangxing Hu* Nanyang Technological University	17:00-17:15
311 **Thermal Resistance Simulation Analysis and Test Research of Wire Bond Ball Grid Array Package** *Fang Qu* State Key Laboratory of Mobile Network and Mobile Multimedia Technology	17:00-17:15	457 **Electrochemical simulation of electrodeposition growth of copper in through silicon via (TSV)** *Zeng-Guang Xu* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS	17:15-17:30
341 **Simulation and Optimization of Large Scale Multiport Power Supply Noise for 2.5D IC** *Chenxi Yang* Sanechips Technology Co., Ltd	17:15-17:30	463 **CPU Socket Interposer Package Level and Interconnect Manufacturability Study-Part 1: Socket Contact vs. Direct-Solder–Attach Interconnection and Part 2: iNEMI 2023 Board Assembly-CPU Socket Technology Roadmap** *Paul Wang* Tyan Computer (a MiTAC company)	17:30-17:45

350 17:30-17:45 **Effects of dishing and annealing temperature on wafer to wafer hybrid bonding** *Yu Li* Wuhan University	

口头报告 19	口头报告 20
地点 会场 5 专题 质量与可靠性 主席 谢 斌 博士	地点 会场 6 专题 新兴领域封装与面向人工智能的电子技术应用 主席 于大全 教授
421 15:30-15:45 **Optimization of packaging process in Ag sintering for ultra-reliable SiC based power electronics** *Minglu Xia* Hong Kong Applied Science and Technology Research Institute, China	**专题特邀报告** 15:30-16:00 **基于玻璃衬底和 TGV 工艺的集成无源器件开发** *阮文彪 博士* 厦门云天半导体科技有限公司研发总监
467 15:45-16:00 **Orientation-related stress analysis of nanotwins copper in redistribution layer for wafer-level packaging** *Ze-Song Wang* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS	233 16:00-16:15 **Nonvolatile Memory Devices Based on Two-Dimensional WSe2/MoS2 van der Waals Heterostructure** *Sixian He* School of Materials Science and Engineering, Shanghai Jiao Tong University
472 16:00-16:15 **Finite Element Simulation Study of the Effects of Kirkendall Voids in IMC Layer on Interfacial Crack and Reliability of Cu–Sn Solder Joints** *Ming-Sheng Luo* South China University of Technology	274 16:15-16:30 **Moisture-responsive Biopolymer Actuators with Programmable Deformation Behavior** *Yunxia Yang* Beijing university of technology
514 16:15-16:30 **Influence of pin position on the CDM peak current based on 2.5D and 2D package** *Menghua Wang* Department of Reliability Engineering, Sanechips Technology Co., Ltd.	276 16:30-16:45 **On-Chip Substrate Integrated Plasmonic Waveguide Bandpass Filter for Millimeter-Wave Applications** *Tian Yu* Xiamen university, School of Electronic Science and Engineering College
526 16:30-16:45 **Effects of Plasma Treatment on Adhesion and Flow Behavior of Underfill in 2.5D electric package** *Yuanyuan Yang* Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences	284 16:45-17:00 **Interfacial Engineering of ZnO/CdS Heterostructure for Long Cycle Life Li-O2 Batteries** *Congcong Dang* School of Materials Science and Engineering, Shanghai Jiao Tong University
528 16:45-17:00 **Electrochemical Migration Mechanism of Cu@Ag Composite Preforms by Electromagnetic Compaction for Power Electronics** *Ziao Li* Wuhan University of Technology	354 17:00-17:15 **Synthesis of Cobalt Doped VSe2 Nanoflake as Cathode Material for Wearable Aqueous Zinc Ion Battery** *Xinxin Wang* State Key Laboratory of Advanced Welding and Joining, Harbin Institute of Technology

533 17:00-17:15 **Correlation Analysis on Warpage and Metal Thermal Interface Materials Thermo-mechanical Reliability of Large size FCBGA** *Zhuolun Wu* State Key Laboratory of Mobile Network and Mobile Multimedia Technology	382 17:15-17:30 **Vertical Hexagonal Arrangement Structure - VHAS** *Akanksha Sahoo* Engineer, Micron
598 17:15-17:30 **Growth behavior of IMC at the Co-P/SAC105/Co-P solder joint interface under Thermoelectric Coupling Fields** *Jing Rong* Chongqing University of Technology	460 17:30-17:45 **Condition monitoring of SiC power module by using time-series analysis of acoustic emission during power cycling tests** *Zheng Zhang* Institute of Scientific and Industrial Research (SANKEN), Osaka University
643 17:30-17:45 **Life Prediction of Solder Interconnects under Harsh Thermal Cycling from Microstructural Degradation** *Wanyu Jiang* State Key Laboratory of Advanced Welding and Joining, Harbin Institute of Technology	

口头报告 21

地点　会场 7

专题　封装材料与工艺

主席　李宇杰 教授

专题特邀报告 15:30-16:00 **基于国产芯片的平面型封装 1700V 碳化硅模块开发与性能表征** *梅云辉 教授* 天津工业大学电气工程学院常务副院长	540 16:45-17:00 **The synthesis and Characterization of well-dispersed submicron copper particles and the research of sintering performance** *Yi Fang* School of Materials Science and Engineering, Harbin Institute of Technology (Shenzhen)
482 16:00-16:15 **Flexible silver/cellulose fabric for highly efficient and broadband EMI shielding via metal-organic decomposition approach** *Si-Yuan Liao* Shenzhen Institute of Advanced Technology Chinese Academy of Sciences	544 17:00-17:15 **Optimization of Wafer-level TTV Using RIE Applied for the Extreme Wafer Thinning** *Jinzhu Li* School of Microelectronics, Fudan University
517 16:15-16:30 **Structural Analysis of Anisotropic Conductive Film for Liquid Crystal Displays and Semiconductor Packaging Applications** *Yadong Xu* Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences	586 17:15-17:30 **Study on Micro-silver Joint Doped with Silicon Carbide Nanowires for Power Electronics** *Mu-lan Li* Sun Yat-sen University
536 16:30-16:45 **Fabrication of Ultra-Thin Conformal Shielding coatings on SiP modules by Inkjet Printing Technology** *Hao Wu* Shenzhen Institute of Advanced Electronic Materials	590 17:30-17:45 **A digital image correlation study on the microstructure and strain behavior of electroplated nanotwinned copper as interconnection material** *Zhiqiang Zhang* Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences

口头报告 22	口头报告 23
地点 会场 1 专题 先进封装 & 封装制造技术与设备 主席 刘 胜 教授	地点 会场 2 专题 封装材料与工艺 主席 高丽茵 博士
专题特邀报告 18:15-18:45 **异构集成封装中几个芯片和封装耦合性问题** *Richard Rao 博士* 美国迈威尔科技资深首席工程师	328 18:15-18:30 **Investigation on Silver Nanowire/Resin-Induced Liquid Crystal Polymer Metallization** *Yongjiang Zhang* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology
238 18:45-19:00 **Scallop-less Nanoscale TSV with F/O Coupling Plasma Etching** *Yang Wang* School of Microelectronics, Fudan University	329 18:30-18:45 **Study on low temperature sintering mechanism and performance of multiscale silver paste** *Yiping Wang* State Key Laboratory of Advanced Welding and Joining, Harbin Institute of Technology
275 19:00-19:15 **High-precision positioning detection technology for large-size panel-level package chips** *Zhihang Chen* School of Electromechanical Engineering, Guangdong University of Technology	333 18:45-19:00 **Green and high-efficiency CMP Slurry for Cu planarization** *Jiale Zhang* Southern University of Science and Technology
324 19:15-19:30 **A New Numerical Algorithm to Estimate the Average Travel Time of Workpiece in Package and Reliability Production Machines** *Niuyi Sun* Sanechips Technology Corporatio	338 19:00-19:15 **Preparation and characterization of submicron silver particles with the nanoscale surface structure for high-reliability packaging** *Bolong Dong* School of Materials Science and Engineering, Harbin Institute of Technology (Shenzhen)
435 19:30-19:45 **Optimization of Laser-induced deep etching for TGV fabrication in fused silica** *Jingli Liu* Southeast University	351 19:15-19:30 **Influence of Bonding Conditions on Low-temperature Solid-state Bonding of Cobalt Based Nanocones** *Silin Han* Shanghai Jiao Tong University
490 19:45-20:00 **Research on AI-Based Gold Removal Technology for Aviation Connector Cup Cavity Surface** *Zhang Yongzhong* Intelligent Electronic Manufacturing Research Center Beijing City University	367 19:30-19:45 **Analysis of Metallization Effects of Pressure-Assisted Cu Nanoparticle Sintering on DBC by Experiment and Nanoscale Simulation** *Shizhen Li* Southern University of Science and Technology
	388 19:45-20:00 **SIP SOLDER PASTE VIA POWDER CLUSTER DESIGN HARVEST BOTH SLUMP RESISTANCE AND TEMPERATURE CYCLING RELIABILITY** *Ning-Cheng Lee* ShinePure Hi-Tech
	338 20:00-20:15 **A Novel High Temperature Resistant Temporary Bonding Material for Ultra-thin Wafer Handling: Superior Room Temperature Bonding, Heat Curing and Mechanical De-bonding Performances** *Kang Li* Shenzhen Institute of Advanced Technology, CAS

	437 20:15-20:30 **The influence of pattern size on the profile and microstructure of electroplated copper pad, redistribution layer and via for advanced packaging** *Jin-Hao Liu* Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences

口头报告 24	口头报告 25
地点 会场 3 专题 封装设计、建模与仿真 主席 刘丰满 教授	地点 会场 4 专题 互连技术 主席 张 昱 教授
400 18:15-18:30 **Die Shift Simulation in Panel Level Packaging** *Bin Gu* ST Microelectronics	471 18:15-18:30 **Effect of soldering temperature on the properties of Cu/SAC0307/Al joints with dual ultrasound assistance** *Yongchong Ma* Chongqing University of Technology
406 18:30-18:45 **Interfacial reliability analysis and structural optimization of System-in-Package module** *Sixin Huang* Huawei Technologies Co., Ltd.	473 18:30-18:45 **An Exploratory Study to Achieve Cu Pillar Direct Bonding with Assistance of Bimodal-sized Cu Nanoparticle Paste by Low-Temperature Thermocompression Bonding in Air** *Li-Ping Wang* South China University of Technology
408 18:45-19:00 **Optimizing conformal shielding scheme with quantitative analysis** *Xinyu Zhang* Microsystem Packaging Research Center, Institute of Microelectronic of Chinese Academy of Sciences	522 18:45-19:00 **Evaluation and Mechanism Study of a Novel Green Chemical Mechanical Polishing Slurry for Cobalt Interconnects** *Zisheng Huang* Shanghai Jiao Tong University
512 19:00-19:15 **Research on Optimized Modeling of Package Warping Phenomenon** *Lin Wu* ChangXin Memory Technologies, Inc.	525 19:00-19:15 **Modeling and Reliability Characterization of Micro-coil Springs for Ceramic Grid Array Integrated Circuits** *Minghua Zhang* Beijing Spacecraft
585 19:15-19:30 **Thermal Stress Field of Al2O3/Al-Ni Nanofoil/Ni Solder Joints by Self-propagation Reactions** *Shengbo Huang* Wuhan University of Technology	599 19:15-19:30 **Design and Fabrication of Flip-chip Interconnection for Superconducting Circuits Based on Silicon Bumps** *Kun Li* Shanghai Institute of Microsystem and Information Technology
626 19:30-19:45 **High-Throughput Screening Modeling for Exploring Low-k Dielectric Constant Crystals** *Zikang Guo* Shanghai Jiao Tong University	610 19:30-19:45 **Wafer-level Sn-Ag-Cu/SiO2 Transient Liquid Phase Hybrid Bonding (TLP-HB) Technology** *Shuai Zhang* Zhejiang Lab, ZJ Lab-Enflame Joint Innovation Research Center

664 19:45-20:00 **Analysis of Complex BGA Transition for Equivalent Circuit Modeling** *Kangrong Li* Xi'an Microelectronics Technology Institute	660 19:45-20:00 **Ultrasonic-accelerated TLPB with Ga-paste Solder for Low-temperature Electronics Interconnects** *Yi Chen* Wolfson School of Mechanical and Manufacturing Engineering Loughborough University, Leicestershire, UK
684 20:00-20:15 **A Lossy Filter Using Quarter-mode Substrate Integrated Waveguide and Coplanar Waveguide** *Shihao Xie* Shanghai university	669 20:00-20:15 **Quantitative Microstructural Data of Bulk Solders and Joints under a New Framework of MicroStructure Hierarchy Descriptor (μSHD)** *Kaiwen Zheng* Sun Yat-sen University
695 20:15-20:30 **Development of Low-Loss and Low-Cost Air-Filled Transmission Lines based on Advanced Glass Wafer-Level Packaging** *Jing Cai* Xiamen University	

口头报告 26	口头报告 27
地点 会场 5 专题 质量与可靠性 & 功率电子与新能源及新型电力系统 主席 鲁 敏 教授	地点 会场 6 专题 新兴领域封装与面向人工智能的电子技术应用 主席 田艳红 教授
671 18:15-18:30 **Simulation on Microstructural Evolution under Electromigration in Backside Power Delivery Network** *Xin Zeng* Sun Yat-sen University	**专题特邀报告** 18:15-18:45 **芯片低温固相互连** *计红军 教授* 哈尔滨工业大学（深圳）
694 18:30-18:45 **Synergistic Effect of Current Stressing and Temperature Cycling on Reliability of Low Melting Point SnBi Solder** *Zesheng Shen* City University of HongKong, China	618 18:45-19:00 **A low power consumption fractal microchannel heat sink based on hierarchical ribs** *Yongjin Wu* Shanghai Jiao Tong University
701 18:45-19:00 **Electromigration behavior study of fine pitch Cu-Sn micro-bump structure by finite element simulation** *Zheqi Xu* School of Integrated Circuits, Tsinghua University	662 19:00-19:15 **Transparent Metal Grid Electrodes Prepared by Electrohydrodynamic Printing Technology** *Jingxuan Ma* Harbin Institute of Technology
709 19:00-19:15 **Application of ANSYS Sherlock in the fatigue lifetime evaluation of board level solder joint** *Mengke Yang* Ericsson BNEW, Ericsson AB, Beijing, China	677 19:15-19:30 **Stealth dicing of SiC using femtosecond laser Bessel beam** *Shaowei Li* Faculty of Materials and Manufacturing, Beijing University of Technology

724 19:15-19:30
Case analysis on the fracture of deformed leads of the ceramic flat package
Zhibin Wang
China Aerospace Components Engineering Center

737 19:30-19:45
Research on Heat Dissipation Technology of GaN Power Amplifier Based on Diamond Carrier
Lixiang Zhang
The 13th Research Institute of CETC

731 19:30-19:45
The crack propagation analysis in an IGBT package under in-service conditions by VCCT
Zhao Fu
Department of Materials Science, Fudan University

736 19:45-20:00
A New Failure Mode Induced by Coupling Effect of Electromigration and Joule Heating in Advanced Packaging
Yifan Yao
City University of Hong Kong, China

443 20:00-20:15
Computational and experimental study of a novel L-cysteine hydrochloride leveler for copper electroplated via fill in redistribution layers
Yu Jiao
Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS

452 20:15-20:30
Ad/desorption mechanism of amine-terminated polyoxypropylene suppressor in advanced acid copper electroplating
Ning Zhang
Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS

口头报告 28

地点 会场 7

专题 封装材料与工艺 & 封装设计、建模与仿真

主席 李财富 教授

629 18:15-18:30
Glycine-Modified Boron Nitride/Epoxy Composites with High Thermal Conductivity and Low Coefficient of Thermal Expansion
Zhen'An Dou
Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences

646 18:30-18:45
Additive fabrication of 3D surface conformal circuits using a modified screen printing technology
Wenbo Li
State Key Laboratory of Advanced Welding and Joining, Harbin Institute of Technology (Weihai)

722	18:45-19:00	
Preparation of Nano-foam sheet and Its Application in High Temperature Resistance Packaging of Power Chips *Hongqiang Zhang* Beihang University		
440	19:00-19:15	
Effects of additive interactions on electroplating profile of IC substrate copper pillars *Xiao Li* Shenzhen Institute of Advanced Electronic Materials, Shenzhen Institute of Advanced Technology, CAS		
442	19:15-19:30	
Prospective application of nanotwinned copper for Damascene via filling and hybrid bonding *Li-Yin Gao* Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences		
717	19:30-19:45	
Low-noise Design for Power Delivery Network in 2.5D Integrated Microsystem *Yanling Wang* Northwestern Polytechnical University / Xi'an Microelectronics Technology Institute		
726	19:45-20:00	
Comparative analysis of different microfluidic cooling technologies for high performance chips *Jianyu Feng* Institute of Microelectronics of the Chinese Academy of Sciences		
730	20:00-20:15	
The prediction of orthotropic material properties for RDL based on effective modeling and CNN *Haozhou Wang* Department of Materials Science, Fudan University		

张贴报告专题

请参考英文版

参会指引

感谢各位嘉宾代表对本次大会的关注与支持，为了更好地为您提供服务，请您留意会务组温馨提示：

1 会议期间参会者请佩戴代表证，并凭此参加各项活动；

2 会议期间用餐时间和地点（代表凭票用餐）；

日期	时间	用餐地点	
8 月 10 日(星期四)	12:20--12:50	茶歇	石河子大学会堂（北区）
	14:10--15:40	午餐	方圆餐厅（北区）
	17:25--17:55	茶歇	石河子大学会堂（北区）
	20:00--22:00	欢迎晚宴	恒和华星酒店
8 月 11 日(星期五)	11:45--12:15	茶歇	博学楼一楼大堂
	14:00--15:30	午餐	方圆餐厅（北区）
	17:45--18:15	茶歇	博学楼一楼大堂

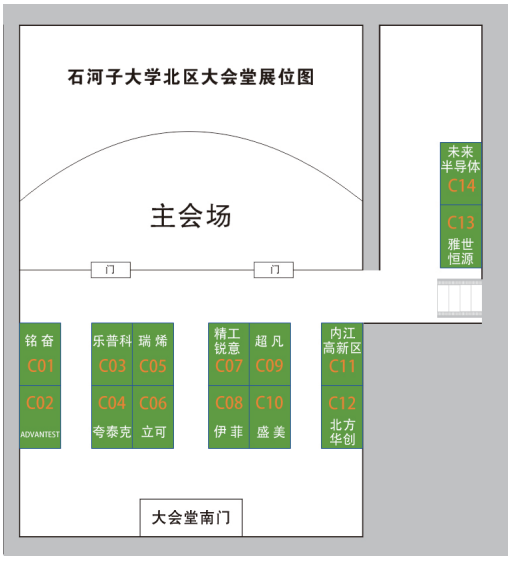
3 请妥善保管好自己随身携带手机、电脑、钱包等贵重物品；

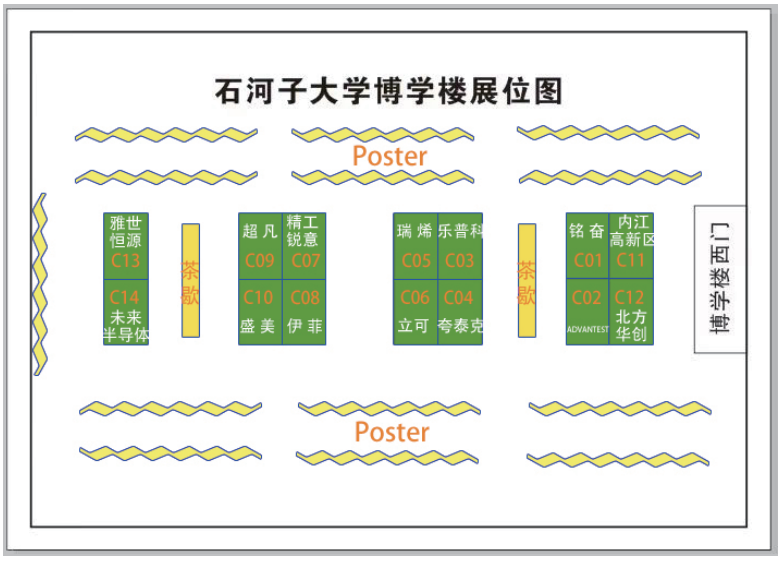
4 住恒和华星酒店的参会代表，请于 8 月 10 日/11 日上午 9:30 于酒店大堂集合，可乘坐专车抵达会场；

5 会议期间的具体安排请查阅会议日程安排，在会场参会的代表，请将手机调成震动状态，请不要大声喧哗，随意走动，请您配合保持良好的会场秩序；

6 展览地点：8 月 10 日 石河子大学会堂南序厅，8 月 11 日 博学楼一楼；

7 论文张贴时间：8 月 9-10 日 10:00--20:00，张贴地点：博学楼一楼；





8 **会务组联系方式**

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王洪坤 Tel: 0086-18099937231 高 攀 Tel: 0086-13179930011

尹 雯 Tel: 0086-010-82995675 施玥如 Tel: 0086-13661508648

石河子恒和华星酒店

杨帆 Tel: 0086-17709930103

·现场注册

可注册地点 1：石河子大学•学术交流中心

（仅限 8 月 8 日）

可注册地点 2：恒和华星酒店

（8 月 8-10 日）

可注册地点 3：石河子大学博学楼

（仅限 8 月 9 日）

备注：

(1) 石河子恒和华星酒店距石河子大学北区南门车程大约 5 分钟；

(2) 石河子爱派国际酒店距石河子大学北区南门车程大约 10 分钟。

·会场布局

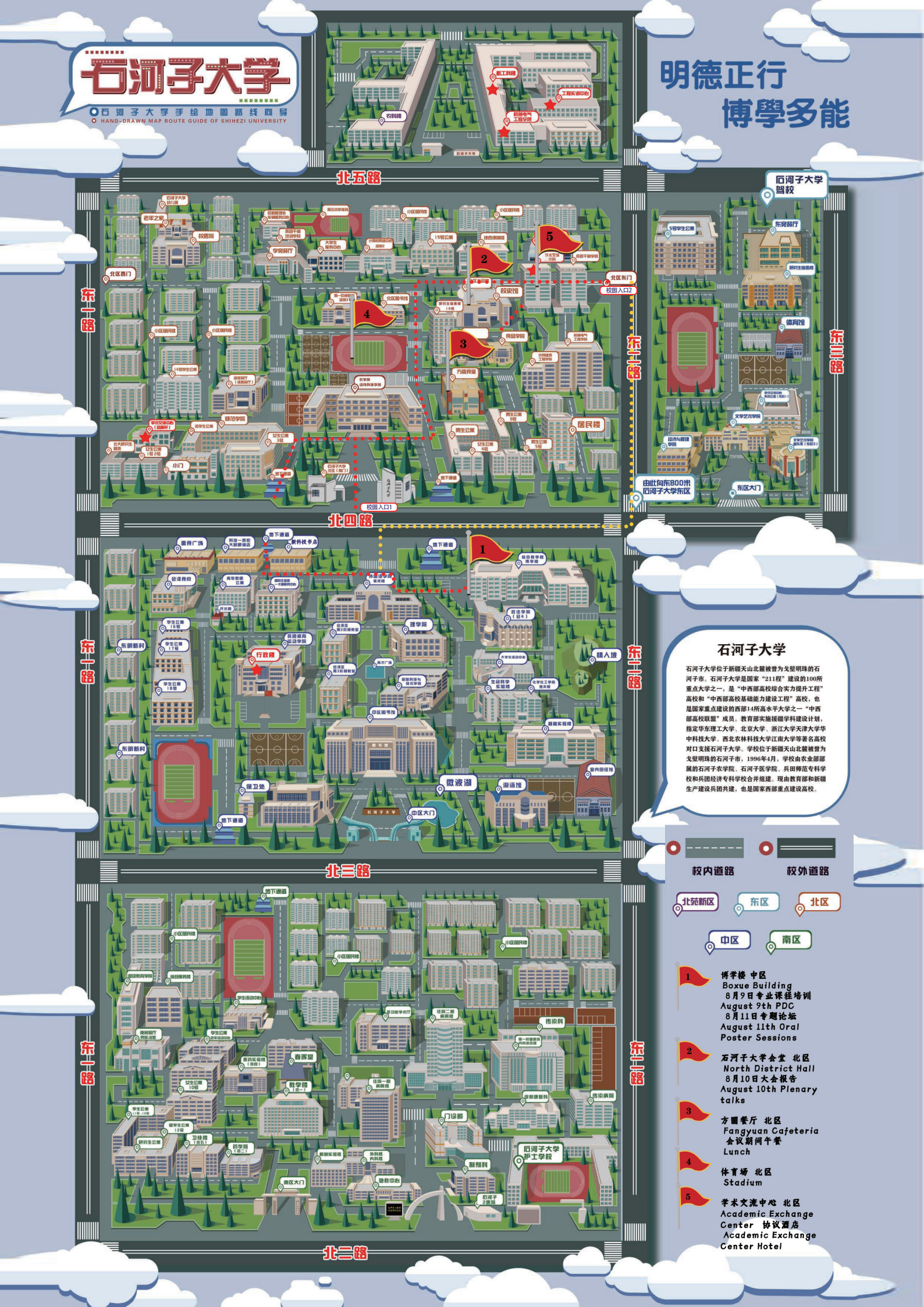
日期	地点	
8 月 9 日（星期三）	专业发展课程培训	石河子大学博学楼（中区）
8 月 11 日（星期五）	专题论坛	
8 月 9 日（星期三）	足球友谊赛	石河子大学体育场（北区）
8 月 10 日（星期四）	开幕式 大会报告	石河子大学会堂（北区）
8 月 10 日（星期四）	欢迎晚宴	恒和华星酒店

石河子大学

石河子大学手绘地图路线图导

HAND-DRAWN MAP ROUTE GUIDE OF SHIHEZI UNIVERSITY

明德正行
博學多能



石河子大学

石河子大学位于新疆天山北麓被誉为戈壁明珠的石河子市。石河子大学是国家“211程”建设的100所重点大学之一，是“中西部高校综合实力提升工程”高校和“中西部高校基础能力建设工程”高校，也是国家重点建设的西部14所高水平大学之一“中西部高校联盟”成员。教育部实施援疆学科建设计划，指定华东理工大学、北京大学、浙江大学天津大学华中科技大学、西北农林科技大学江南大学等著名高校对口支援石河子大学。学校位于新疆天山北麓被誉为戈壁明珠的石河子市，1996年4月，学校由农业部部属的石河子农学院、石河子医学院、兵团师范专科学校和兵团经济专科学校合并组建。现由教育部和新疆生产建设兵团共建，也是国家西部重点建设高校。

1 博学楼 中区
Boxue Building
8月9日专业课程培训
August 9th PDC
8月11日专题论坛
August 11th Oral Poster Sessions

2 石河子大学会堂 北区
North District Hall
8月10日大会报告
August 10th Plenary talks

3 方圆餐厅 北区
Fangyuan Cafeteria
会议期间午餐
Lunch

4 体育场 北区
Stadium

5 学术交流中心 北区
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- 晶圆到晶圆(W2W)和晶片到晶圆(D2W)混合键合工艺已为样品测试、产品开发和鉴定做好准备
- 面向整个微电子供应链的EVG客户和合作伙伴开放创新孵化器、确保严格执行知识产权保护标准
- 结合EVG先进的晶圆键合、薄型晶圆处理和无掩模、光学和纳米压印光刻产品和专业技术，以及试生产设施和服务

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天津工業大學
TIANGONG UNIVERSITY

天津工业大学始建于1912年， 坚持“工科做强、理科做优、文科做精、医科做好”的发展思路，坚持以德为先、能力为重、全面发展和个性发展相结合的原则，坚持立德树人，坚持为党育人、为国育才，坚持改革创新，着力培养胸怀经纬、求真务实、品高学优、工勤业精、具有高度社会责任感、创新精神和实践能力的高级专门人才，形成了以工为主、多学科统筹发展的良好学科生态布局。学校拥有包括中国工程院院士等国家级高层次人才60余名，省部级各类人才200余名，拥有全国首批高校黄大年式教师团队、国家级教学团队、教育部创新团队等省部级及以上高层次团队40余支，入选国家级创新人才培养示范基地。2017年、2022年连续进入国家“双一流”建设高校序列。

天津工业大学具有较强的科研实力和科技成果转化能力，鼓励自主创新，彰显现代纺织和国防军工特色，建有国家级实验室1个，国家级研究中心3个，省部级实验室10个，省部级研究中心8个，省部级工程中心6个。近年来承担了“973”计划、“863”计划、国家重点研发计划项目（课题）、国家社会科学基金项目、国家自然科学基金项目以及有关省部级各类科研课题近千项，并取得多项标志性和突破性成果，连续九年蝉联11项、累计获得国家科技奖14项，获授权专利1000余项，形成了特色科研优势，多项科研成果打破国际垄断，应用于重大疫情防控、国家战略性新兴产业和国防高科技产业。

近年来，以国家在新材料、智能制造、能源、信息和交通等领域中的战略需求为导向，针对大功率高密度器件在照明、汽车、军工和电力等领域的实际问题，围绕材料、器件及功能化设计、系统应用集成技术开展研究。突出大功率高密度器件应用技术特色，形成材料设计-器件制备-应用系统-智能集成的创新研究链和全链条人才梯队；培养和凝聚该领域杰出人才和优秀研究群体，为国家和京津冀区域重大战略服务。